TELECOMMUNICATION
SPEECH
A/D-CONVERTER
COMPONENTS

Contents

μPD22100C
4x4 CROSSPOINT SWITCH WITH CONTROL MEMORY

4 x 4 CROSSPOINT SWITCH WITH CONTROL MEMORY
CMOS

The μPD22100C consists of 16 crosspoint switches organized in 4 rows and 4 columns. Any of the 16 Switches can be selected by applying its address to the device and pulse to the strobe input. The selected crosspoint will turn on if during strobe, Data In was a one and will turn off if during strobe, Data In was a zero. Other switches are unaffected. On internal power-on reset turns off all-switches as power is applied.

Truth Table

INPUTS						SELECTED CHANNELS															
S	D	C	B	A	D	$^{Y}X0$	$^{Y}X1$	$^{Y}X2$	$^{Y}X3$	$^{Y}X0$	$^{Y}X1$	$^{Y}X2$	$^{Y}X3$	$^{Y}X0$	$^{Y}X1$	$^{Y}X2$	$^{Y}X3$	$^{Y}X0$	$^{Y}X1$	$^{Y}X2$	$^{Y}X3$
L	x	x	x	x	x	NC	→														
H	L	L	L	L	L	OFF	NC	→													
H	L	L	L	L	H	ON	NC	→													
H	L	L	L	H	L	NC	OFF	NC	→												
H	L	L	L	H	H	NC	ON	NC	→												
H	L	L	H	L	L	NC	→	OFF	NC	→											
H	L	L	H	L	H	NC	→	ON	NC	→											
H	L	L	H	H	L	NC	→		OFF	NC	→										
H	L	L	H	H	H	NC	→		ON	NC	→										
.	.	.	.	.	.	.															.
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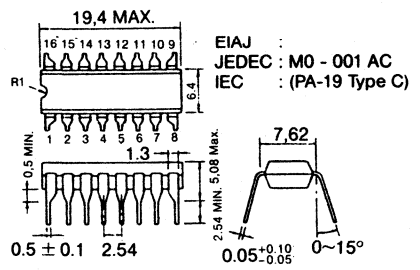
.	.	.	.	.	.	.															.
H	H	H	H	H	L	NC	→														OFF
H	H	H	H	H	H	NC	→														ON

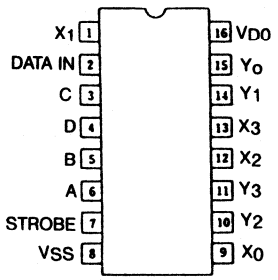
L : Low Level, H : High Level, NC : No Change, x : L or H

Package Dimensions (Unit : mm)

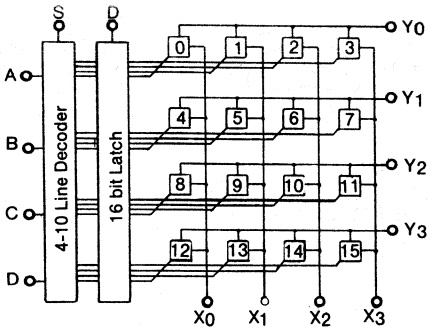


EIAJ :
JEDEC : M0 - 001 AC
IEC : (PA-19 Type C)

Connection Diagram (Top View)



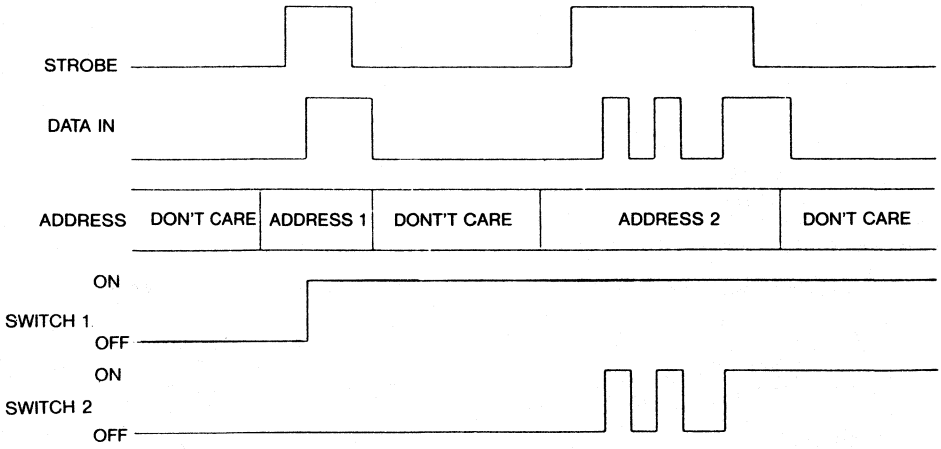
Block Diagramm



S : Strobe
D : Data in

n : Analog Switch

Timing Chart



Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Absolute Maximum Ratings	Unit
DC Supply Voltage	V_{DD}	−0.5 ~ +20	V
Input Voltage	V_I	−0.5 ~ V_{DD} + 0.5	V
Input Current	I_I	10	mA
Power Dissipation	P_D	200	mW
Operating Temp.	T_{opt}	−40 ~ +85	°C
Storage Temp.	T_{stg}	−65 ~ +125	°C

Recommended Operating Conditions (Ta = −40 / + 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}		3		18	V
Input Voltage	V_{IH}		0.7V_{DD}		V_{DD}	V
Input Voltage	V_{IL}		0		0.3V_{DD}	V
Analog Input Volt	V_{IA}		V_{SS}		V_{DD}	V

Electrical Characteristics

Item		V_{DD}(V)	Conditions	Ta = −40°C Min.	Ta = −40°C Max.	Ta = 25 °C Min.	Ta = 25 °C Typ.	Ta = 25 °C Max.	Ta = + 85°C Min.	Ta = + 85°C Max.	Unit
On-State Resistance	R_{ON}	5	$V_{IS} = \frac{V_{DD} - V_{SS}}{2}$		1000		225	1250		1440	Ω
		10			145		85	180		200	
		12			110		75	135		165	
		15			75		65	95		110	
On-State Resistance Difference Between Any Two Switches	ΔR_{ON}	5	$V_{IS} = \frac{V_{DD} - V_{SS}}{2}$				35				Ω
		10					20				
		12					18				
		15					15				
Input Leakage Current	I_L	18	All Switches OFF		±100		±1	±100		±10000	nA
Input Voltage (Logic)	V_{III}	5	Switch ON $R_{ON} < R_{ON}$ Max.	3.5		3.5			3.5		V
		10		7		7			7		
		15		11		11			11		
Input Voltage (Logic)	V_{II}	5	Switch OFF $I_L < 0.2$ μA		1.5			1.5		1.5	V
		10			3			3		3	
		15			4			4		4	
Input Current	I_I	18	$V_I = V_{SS}, V_{DD}$		±0.1		$\pm 10^{-3}$	±1		±1	μA
Quiescent Current	I_{DD}	5	$V_I = V_{SS}, V_{DD}$		5		0.04	5		150	μA
		10			10		0.04	10		300	
		15			20		0.04	20		600	
		20			100		0.08	100		3000	

Switching Characteristics (Ta = 25 °C)

Characteristics	Symbol	V_{DD}(V)	Conditions		Min.	Typ.	Max.	Unit
Propagation	t_{PLH} t_{PHL}	5	Signal INPUT → Signal OUTPUT R_L = 10 kΩ, C_L = 50 pF $t_r = t_f$ = 20 NS			30	60	ns
		10				15	30	
		15				10	20	
	t_{PZH}	5	Strobe INPUT → OUTPUT	R_l = 1 kΩ C_L = 50 pF L_r, t_l = 20 ns		300	600	ns
		10				125	250	
		15				80	160	
	t_{PZH}	5	Data INPUT → OUTPUT			110	220	ns
		10				40	80	
		15				25	50	
	t_{PZH}	5	Address INPUT → OUTPUT			350	700	ns
		10				135	270	
		15				90	180	
	t_{PHZ}	5	Strobe INPUT → OUTPUT			165	330	ns
		10				85	170	
		15				70	140	
	t_{PLZ}	5	Data INPUT → OUTPUT			210	420	ns
		10				110	220	
		15				100	200	
	t_{PHZ}	5	Address INPUT → OUTPUT			435	870	ns
		10				210	420	
		15				160	320	
Set Up Time	$t_{set\ up}$	5	Data INPUT → Strobe Address			95	190	ns
		10				25	50	
		15				15	30	
Hold Time	t_{hold}	5	Data INPUT → Strobe INPUT Address INPUT			180	360	ns
		10				110	220	
		15				35	70	
Frequency	$f_{\phi max}$	5	R_L = 1 kΩ, C_L = 50 pF t_r, t_f = 20 ms		0.6	1.2		MHz
		10			1.6	3.2		
		15			2.5	5		
Strobe Pulse Width	t_w (STROBE)	5				300	600	ns
		10				120	240	
		15				90	150	
Crosstalk Voltage		10	R_L = 10 kΩ $t_r = t_f$ = 20 ns Rectronglar			75		mV (peak)
INPUT Capacitance	C_{IN}		Data, Strobe, Address INPUT			5	7.5	pF
Feedthrough Capacitance			Signal INPUT	Xn		30		pf
				Yn		30		
	$C_{IN/OUT}$					0.4		pF

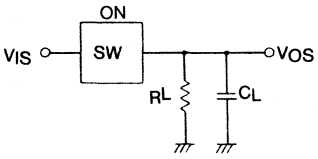
Switching Time Characteristics (Ta = 25°C)

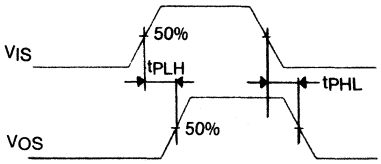
Characteristics	Symbol	V_{DD}(V)			Min.	Typ.	Max.	Unit
Frequency Response (Switch on)	–	10	R_L = 1 kΩ, V_{IS} = 5 $V_{(P-P)}$ 20 log $\frac{V_{OS}}{V_{IS}}$ = – 3 dB			40		MHz
Feedthrough Attenuation (Switch Off)	–	10	R_L 1 kΩ, f = 1.6 kHz, V_{IS} = 5 V (P-P) Sine Wave Input			–80		dB
Sine Wave Distortion	–	10	R_1 = 1 kΩ, V_{IS} = 5 V (P-P) f = 1kHz			0.5		%
Crosstalk Between Any Two Switches	–	10	R_L = 1 kΩ SW (A) = ON SW (B) = OFF	20 log $\frac{V_0\ (B)}{V_I\ (A)}$ = –40dB		1.5		MHz
				20 log $\frac{V_0\ (B)}{V_I\ (A)}$ = –110dB		0.1		kHZ

TEST CIRCUITS

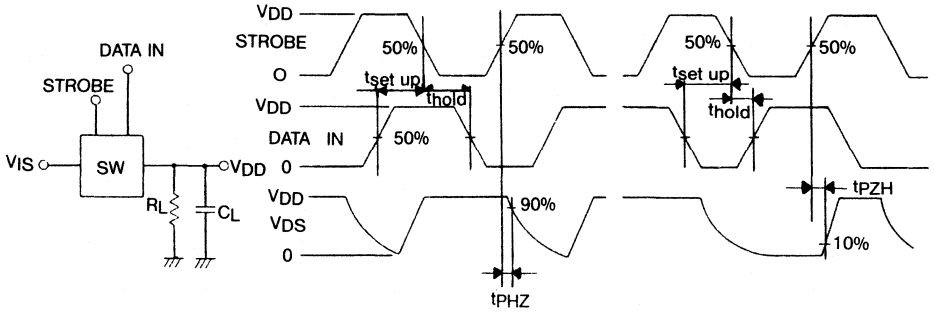
□ PROPAGATION DELAY TIMES

(1) SIGNAL INPUT → SIGNAL OUTPUT





(2) STROBE INPUT → OUTPUT



μPD9513D/9514D
PCM COMBO

μPD951X Familiy Lineup

Type	Com-panding law	Signaling	Clock			Input AMP	Test Capability	Package
			SYNC/ ASYNC Operation	Fixed Data Rate Mode	Variable Data Rate Mode			
μPD9514D	A or μ	Sign.	Sync/ Async	1,536 or 1,544 or 2,048 Mbps	64 K to 2,048 Mbps Non-Sign.	Inverting or Non-Inv.	● analog loop back ● Xmit encoder ● Rcv & Xmit Filter	24 pin Cer DIP
μPD9513D	A or μ	Non-Sign.	Sync only	1,536 or 1,544 or 2,048 Mbps	64 K to 2,048 Mbps	Inverting or Non-Inv.	● Xmit encoder ● Rcv & Xmit Filter	20 pin Cer DIP
μPD9516D	μ	Non-Sign.	Sync only	2,048 Mbps only	64 K to 2,048 Mbps	Inverting only	None	16 pin Cer DIP
μPD9517D	A	Non-Sign.	Sync only	2,048 Mbps only	64 K to 2,048 Mbps	Inverting only	None	16 pin Cer DIP

The μPD9513 D and μPD9514D are single-chip PCM CODEC (COMBO) LSIs with transmit/receive filters. The μPD9514D transmit/receive channel is capable of asynchronous operation, so its application is ideal to D3/D4 type channel banks and subscriber carrier systems. The μPD9513D does not work asynchronously, and the number of pins it has is reduced to 20. Therefore, suitable applications for it are in PBX's and central office switching systems where synchronous operation and high-density mounting are required.

These CODEC LSIs have wide dynamic ranges. Therefore, in addition to use in communication systems, they can be used in various applications such as digital processing of voice signals.

Features

- These are complete single-chip PCM CODECs (COMBO) LSIs with the following circuits internally provided:
- Transmit channel input operational amplifier
- Transmit channel RC-active LPF and switched capacitor HPF/LPF
- μ-law/A-law compatible coder and decoder
- Autozero circuit
- Receive channel switched-capacitor LPF
- Receive channel balanced output power amplifier
- High-accuracy reference voltage circuit
- Serial I/O interface circuit
- μ-law/A-law mode setting by pin connection
- Two types of data transmission modes
  Fixed data rate (1.536/1.544/2.048MHz selectable)
  Variable data rate (64Kbps to 2.048 Mbps)
- Balanced/unbalanced output power amplifier capable of directly driving a 600Ω load is internally supported as a receive output amplifier
- Low power consumption
  80 mW TYP. in normal operation
  8 mW TYP. in power-down mode
- Capable of asynchronous operation of transmit/receive channel*
- Internally provided signaling function*
- Internally provided analog loopback test function*
- Single-chip CMOS monolithic LSI
- 24-pin ceramic DIP*
- 20-pin ceramic DIP**
- 9513AD/9514AD same specification as 9513D/9514D but latch up free

* Provided in μPD9514D only
** Provided in μPD9513D only

Note: Parameters exceeding the values specified in the following tables, should be filled-in by each customer in the specially reserved columns (Customer specification) and returned to NEC.
Additional information needed:

Date : _____

Customer Name : _____

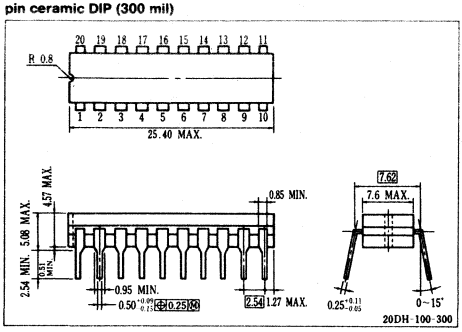
Potential Quantity : _____

Project Timing : _____

Package Dimensions (Unit: mm)

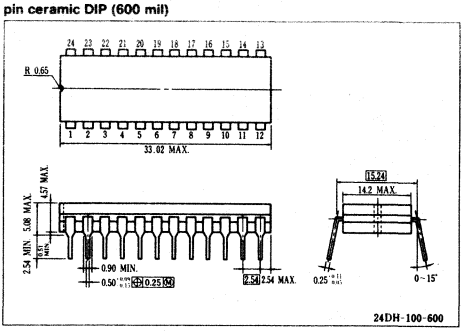
μPD9513D

pin ceramic DIP (300 mil)



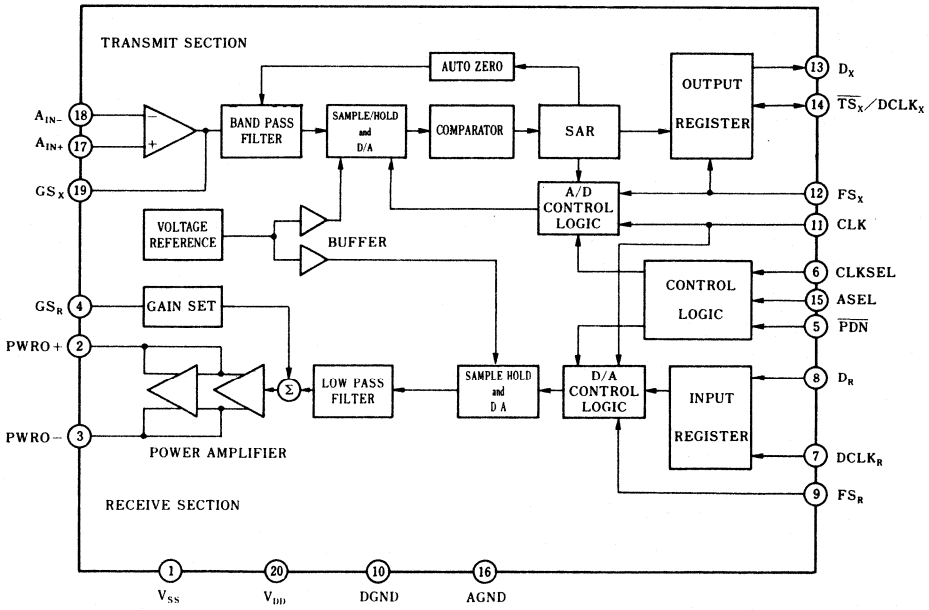
μPD9514D

pin ceramic DIP (600 mil)

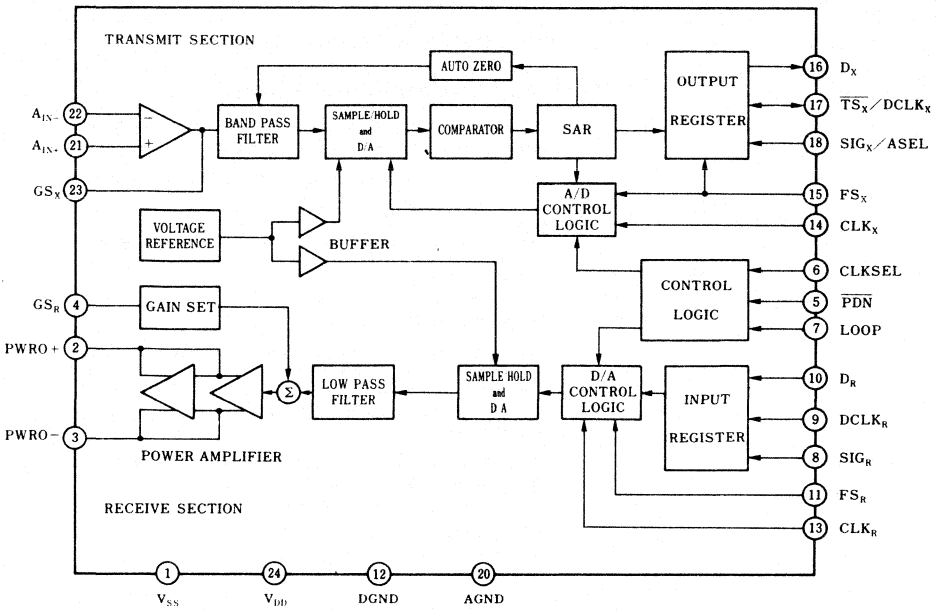


Block Diagrams

μPD9513D

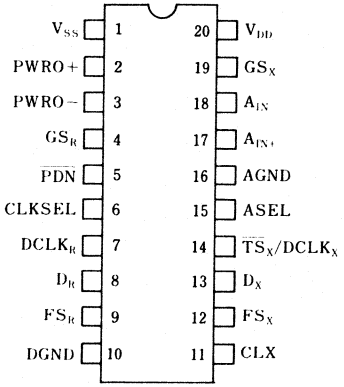


μPD9514D

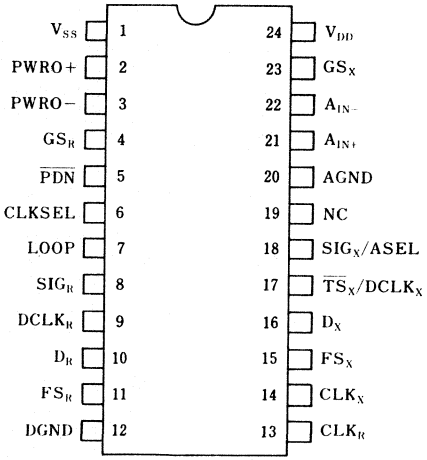


Pin Connections

μPD9513D



μPD9514D



Pin No. μPD9513D	Pin No. μPD9514D	Symbol	Input/ Output	Function
1	1	V_{SS}	--	Negativ supply: input voltage is - 5V ± 0.25V.
2	2	PWRO+	Output	Non-inverting output of receive power amplifier. Can directly drive 600Ω load (in a differential configuration).
3	3	PWRO-	Output	Inverting output of receive power amplifier. Functionally identical and complementary to PWRO+.
4	4	GS_R	Input	Input to the gain setting network of the output power amplifier.
5	5	$\overline{PDN}$	Input	Power-down select (active low).
6	6	CLKSEL	Trivalue input	Input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. f_{CLK} = 2.048 MHz . . . to V_{SS} f_{CLK} = 1.544 MHz . . . to DGND f_{CLK} = 1.536 MHz . . . to V_{DD}
--	7	LOOP	Input	Analog loopback control input (active high). When this pin is active, PWRO+ is internally connected to AIN+ pin, GS_R is internally connected to PWRO-, and AIN- is internally connected ot GS_X. A 0 dBm0 digital signal input at D_R is returned as a +3dBm0 digital signal output at D_X.
--	8	SIG_R	Output	Signaling bit output, receive channel. SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame to which two data clock widths of FS_R are added.
7	9	$DCLK_R$	Input	Selects fixed or variable data rate mode. ● When $DCLK_R$ is connected to V_{SS}, fixed data rate mode is selected. ● When $DCLK_R$is not connected to V_{SS}, variable mode is in effect. In this mode, $DCLK_R$ becomes the receive data clock which operates at 64Kbps to 2.048 Mbps.
8	10	D_R	Input	Receive PCM input. 8-bit PCM data are clocked in on this lead for eight consecutive falling edges of the receive data clock: CLK_R for fixed data rate mode, and $DCLK_R$ for variable data rate mode.
9	11	FS_R	Input	8kHz frame synchronization clock input, receive channel. ● In fixed data rate mode, distinguishes between signaling and nonsignaling frames by means of a double- or single-wide pulse, respectively (μPD9514D). ● In variable data rate mode, this signal must remain high for the entire length of the timeslot. Receive channel enters the standby state whenever this pin is held low for 300ms.
10	12	DGND	--	Digital ground. Not internally tied to analog ground.
--	13	CLK_R	Input	Receive master clock pin. Receive master and data clock for the fixed data rate mode (in variable data rate mode, receive master clock only).
11	14	CLK/CLK_X	Input	Transmit master clock pin. Transmit master and data clock for the fixed data rate mode (in variable data rate mode, transmit master clock only)
12	15	FS_X	Input	8kHz frame synchronization clock input, transmit channel. ● In fixed data rate mode, distinguishes between signaling and nonsignaling frames by single- and double-wide pulses, respectively (μPD9514D). ● In variable data mode, this signal must remain high for the entire length of the timeslot. Transmit channel enters the standby state whenever this pin is held low for 300 ms.

Pin No. μPD9513D	Pin No. μPD9514D	Symbol	Input/ Output	Function
13	16	D_X	Input	Transmit PCM output. 8-bit PCM data are clocked out on this lead for eight consecutive rising edges of the transmit data clock: CLK_X in fixed data rate mode, and $DCLK_X$ in variable data rate mode.
14	17	$\overline{TS_X}$/ $DCLK_X$	Output/ Input	Transmit channel timeslot strobe output or data clock input for the transmit channel. ● In fixed data rate mode, this pin is an open drain output, and the transmit channel strobe signal is output. ● In variable data rate mode, this pin becomes the transmit data clock input pin which operates at 64bps to 2.048Mbps.
15	18	SIG_X/ ASEL	Input	Dual-purpose pin which selects transmit signaling input or A-law. ● When connected to V_{SS}, A-law operation is selected. ● When not connected to V_{SS}, μ-law operation is selected, and this pin becomes the transmit signaling input pin. This input is transmitted at the eighth bit of the signaling frame.
--	19	NC	--	No connect
16	20	AGND	--	Analog ground pin. Not internally connected to digital ground.
17	21	AIN+	Input	Transmit non-inverting analog input pin.
18	22	AIN-	Input	Transmit inverting analog input pin.
19	23	GS_X	--	Transmit operational amplifier output pin. Internally connected to the filter of the next stage.
20	24	V_{DD}	--	Positive power supply: + 5 ± 0.25V.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Parameter/Conditions	Rating	Unit	Customer Spec. Rating
Supply Voltage	V_{DD}		-0.3 to +7.0	V	
	V_{SS}		-7.0 to +0.3		
Analog Input Voltage	V_{AIN}	AIN+, AIN−, GS_R, GS_X	V_{SS} -0.3 to V_{DD} +0.3	V	
Digital Input Voltage	V_{DIN1}	For pins other than CLKSEL, $DCLK_R$, SIG_X/ASEL	-0.3 to V_{DD} +0.3	V	
	V_{DIN2}	CLKSEL, $DCLK_R$, SIG_X/ASEL pins	V_{SS} -0.3 to V_{DD} +0.3		
Voltage Applied to Digital Output Pin	V_{DOUT}	For all digital output pins	-0.3 to V_{DD} +0.3	V	
Power Dissipation	P_T		500	mW	
Operating Temperature	T_{opt}		0 to +70	°C	
Storage Temperature	T_{stg}		-65 to +150	°C	
Soldering Temperature	T_{sold}	Less than 10 seconds	+260	°C	

Note: All voltages are based on the condition that $V_{DG} = V_{AG} = 0$, unless otherwise specified.
It should be connected to Analog ground with shorting at the just under position of IC between AGND and DGND pins.

Recommended Operating Conditions

V_{DD} = +5 ± 0.25V, V_{SS} = −5 ± 0.25V, $V_{DG} = V_{AG} = 0$,
$0 \leqq T_a \leqq 70°C$, unless otherwise specified

(1) D.C. Conditions

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer spec. Min.	Typ	Max.
Supply Voltage	V_{DD}			+4.75		+5.25	V			
	V_{SS}			-5.25		-4.75				
Load Resistance	RL_{AX}	Transmit amplifier		10			kΩ			
Load Capacitance	CL_{AX}					50	pF			
Load Resistance	RL_{AR}	Receive amplifier	Unbalanced output	300			Ω			
			Balanced output	600						
Load Capacitance	C_{LAR}		PWRO+, PWRO- pins			100	pF			
Input Low Voltage	V_{IL}	Digital input pins other than CLKSEL Pin (See Note)		0		0.8	V			
Input High Voltage	V_{IH}			2.0		V_{DD}				
Input Low Voltage	V_{ILO}	CLKSEL pin	f_{CLK} 2.048MHz	V_{SS}		V_{SS}+0.5	V			
Input Intermediate Voltage	V_{IIO}		f_{CLK} = 1.544MHz	V_{DG}-0.5		V_{DG}+0.5				
Input High Voltage	V_{IHO}		f_{CLK} = 1.536MHz	V_{DD}-0.5		V_{DD}				

Note: When $DCLK_R$ pin is connected to V_{SS} pin, the fixed data rate mode is selected.

(2) Clock

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
Master Clock Frequency	f_{CLK} (1/tcy)	When CLKSEL is connected to V_{DD}		1.536		MHz			
		When CLKSEL is connected to DGND		1.544					
		When CLKSEL is connected to V_{SS}		2.048					
Master Clock Duty Cycle	t_{CDC}		45	50	55	%			
Data Clock Frequency	f_{DCLK} ($1/t_{DCY}$)		64		2048	kHz			
Master Clock Pulse Width	t_{CLK}		220			ns			
Frame sync Frequency	f_{FS}		7.9996	8.0000	8.004	kHz			
D_R Setup Time	t_{DSR}		10			ns			
D_R Hold Time	t_{DHR}		60						
Frame Sync Delay Time	t_{FSD}		100		t_{CY} - 100	ns			
Clock Rise Time	t_r				30	ns			
Clock Fall Time	t_f				30				

(3) Timing In Fixed Data Rate Mode

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
SIG x Setup Time	t_{SS}	**μPD9514D**	0			ns			
SIG x Hold Time	t_{SH}		0						

(4) Timing In Variable Data Rate Mode

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
Timeslot Delay Time	t_{TSD}	Referenced to $DCLK_X$, $DCLK_R$	140		t_{DCY}-140	ns			
Frame Sync Delay Time	t_{FSD}		100		t_{CY}-100	ns			
Data Clock Pulse Width	t_{DCW}		220			ns			
Time slot Hold Time	t_{TSH}		0			ns			

Note: $t_{DCY} = 1/f_{DCLK}$, $t_{CY} = 1/f_{CLK}$

64 KB Operation, Variable Data Rate Mode

Item	Symbol	Parameter/Conditions	Min.	Typ	Max.	Unit	Customer Spec. Min.	Typ	Max.
Transmit Frame Sync. Minimum Downtime	t_{FSLX}	FS_X is TTL high for remainder of frame	488			ns			
Receive Frame Sync Minimum Downtime	t_{FSLR}	$FS_R$is TTL high for remainder of frame	1952			ns			
Data Clock Pulse Width	t_{DCW}				10	μs			

D.C. Electrical Characteristics

$0 \leqq T_a \leqq 70°C$, $V_{DD} = +5 \pm 0.25V$, $V_{SS} = -5 \pm 0.25V$,
$V_{DG} = V_{AG} = 0$, $fDCLX_R = fDCLK_X = 2.048MHz$
All outputs unloaded unless otherwise specified
Typical values are for $T_a = 25°C$, $V_{DD} = +5V$, and $V_{SS} = -5V$

(1) Power Dissipation

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Typ	Customer Spec. Max.
Operating Current	I_{DD}	In normal operation		8.0	13.0	mA		
	$\lvert I_{SS} \rvert$			8.0	13.0			
Power-Down Current	I_{DDPD}	$\overline{PDN}$ pin is set to low after 10μs		0.8	1.3			
	$\lvert I_{SSPD} \rvert$			0.8	1.0			
Standby Current	I_{DDST}	FS_X and FS_R are set to low after 300 ms		0.8	1.3			
	$\lvert I_{SSST} \rvert$			0.8	1.0			
Operating Power Dissipation	P_D	In normal operation		80	136.5	mW		
Power-Down Dissipation	P_{DPD}	$\overline{PDN}$ pin is set to low after 10μs		8	12.1			
Standby Power Dissipation	P_{DST}	FS_X and FS_R are set to low after 300 ms		8	12.1			

(2) Digital Interface

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Typ	Customer Spec. Max.
Digital Input Current	$I_{ID}1$	$O \leqq V_{DIN} \leqq V_{DD}$			10	μA			
	$I_{ID}2$	CLKSEL and $DCLK_R$ SIG_X/ASEL pins $V_{SS} \leqq V_{DIN} \leqq V_{DD}$			10				
Output Low Voltage	V_{OL}	D_X, $\overline{TS_X}$, and SIG_R pins $I_{OL} \leqq 3.2mA$			0.4	V			
Output High Voltage	V_{OH}	D_X pin ($I_{OH} \leqq 9.6mA$) SIG_R pin ($I_{OH} \leqq 1.2mA$)	2.4						
Digital Output Capacitance	C_{OD}			5		pF			
Digital Input Capacitance	C_{ID}				10				

(3) Transmit Amplifier

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Input Leakage Current	I_B	$-2.17 \leqq V_{AIN} \leqq 2.17$ V, AIN^+, AIN-			100	nA		
Input Resistance	R_{IN}		10 000			kΩ		
Input Offset Voltage	V_{IO}		-25		25	mV		
Common Mode Rejection	CMRR	$-2.17 \leqq VAIN \leqq 2.17V$	55			dB		
Voltage Gain	A_V		5 000					

(4) Receive Power Amplifier

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
Output Offset Voltage	V_{OS}	Unbalanced output connection, PWRO+ and PWRO- pins	-150	-75	150	mV			
Output Reisistance	R_{ORR}	PWRO+, PWRO-		1		Ω			

A.C. Electrical Characteristics

$0 \leqq T_a \leqq 70°C$, $V_{DD} = 5 \pm 0.25V$, $V_{SS} = -5 \pm 0.25V$
$V_{DG} = V_{AG} = 0$,

(1) Timing Parameters in Fixed Data Rate Mode

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Max.
Data Enable Delay	t_{DZX}	CL < 100pF	0		145	ns		
Data Delay	t_{DDX}	CL < 100pF	0		145	ns		
Data Hold Time	t_{HZX}	CL = 0	60		220	ns		
TS_X Enable Delay	t_{SON}	CL < 100pF	0		145	ns		
TS_X Disable Delay	t_{SOFF}	CL = 0	50		210	ns		
SIG_R Update Time	t_{SIGR}		0		2	μs		

(2) Timing Parameters in Variable Data Rate Mode

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Max.
D_X Active Delay	t_{DON}	CL < 100pF	0		65	ns		
D_X Inactive Delay	t_{DOFF}	CL < 100 pF	0		90	ns		
Data Delay	t_{DFSX}		0		140	ns		
Data Delay	t_{DDX}	CL < 100pF	0		100	ns		

Transmission Characteristics

Ta = 25°C, V_{DD} = 5±0.25V, V_{SS} = 5±0.25V, $\overline{V}_{AG} = \overline{V}_{DG} = 0$,
analog input signal level Vin = 0 dBm0 (f = 1020Hz),
analog input operational amplifier gain = 1 (non-inverting),
digital input signal level 0 dBm0 (f = 1020Hz),
receive output power amplifier gain = 1,
unbalanced output (PWRO+), unless otherwise specified.

(1) Gain Characteristics

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Encoder Milliwatt Response (Transmit gain tolerance)	EmW	V_{DD} = 5 V V_{SS} = -5 V	-0.15		+0.15	dBm0		
EmW Variation with Temp. and Power Supply	EmW_{TS}	0 ≦ Ta ≦ 70°C V_{DD} = 5±0.25V V_{SS} = -5±0.25V	-0.12		+0.12	dB		
Digital Milliwatt Response (Receive Gain Tolerance)	DmW	Measure relative to $OTLP_R$. Signal input per CCITT recommendation G.711. Output signal of 1000Hz. V_{DD} = 5 V, V_{SS} = -5V	-0.15		+0.15	dBm0		
DmW Variation with Temp. and Power Supply	DmW_{TS}	0 ≦ Ta ≦ 70°C V_{DD} = 5±0.25V V_{SS} = -5±0.25V	-0.08		+0.08	dB		

Zero Transmission Level Points

Item	Symbol	Parameter/Conditions	Value	Unit	Customer Spec.
Zero Transmission Level Point Transmit Channel (μ-law)	$OTLP1_X$	Referenced to 600Ω	+2.76	dBm	
		Referenced to 900Ω	+1.00		
Zero Transmission Level Point Transmit Channel (A-law)	$OTLP2_X$	Referenced to 600Ω	+2.79	dBm	
		Referenced to 900Ω	+1.03		
Zero Transmission Level Point Receive Channel (μ-law)	$OTLP1_R$	Referenced to 600Ω	+5.76	dBm	
		Referenced to 900Ω	+4.00		
Zero Transmission Level Point Receive Channel (A-law)	$OTLP2_R$	Referenced to 600Ω	+5.79	dBm	
		Referenced to 900Ω	+4.03		

(2) Gain Tracking (Variation of gain with input level)
(Reference level = 10dBm0, unless otherwise specified)

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
Transmit Gain Tracking Error 1	$GT1_X$	μ-law CCITT G. 712 Method 2	+ 3 to -40dBm0	-0.25		+0.25	dB			
			-40 to -50dBm0	-0.5		+0.5				
			-50 to -55dBm0	-1.2		+1.2				
Transmit Gain Tracking Error 2	$GT2_X$	A-law CCITT G. 712 Method 2	+ 3 to -40dBm0	-0.25		+0.25	dB			
			-40 to -50dBm0	-0.5		+0.5				
			-50 to -55dBm0	-1.2		+1.2				
Transmit Gain Tracking Error 3	$GT3_X$	A-law white noise input CCITT G. 712	-10 to -55dBm0		-0.1		dB			
			-55 to -60dBm0		-0.3					
Receive Gain Tracking Error 1	$GT1_R$	μ-law CCITT G. 712 Method 2 R_L=300Ω PWRO+	+ 3 to -40dBm0	-0.25		+0.25	dB			
			-40 to -50dBm0	-0.5		+0.5				
			-50 to -55dBm0	-1.2		+1.2				
Receive Gain Tracking Error 2	$GT2_R$	A-law CCITT G. 712 Method 2 R_L=300Ω PWRO+	+ 3 to -40dBm0	-0.25		+0.25	dB			
			-40 to -50dBm0	-0.5		+0.5				
			-50 to -55dBm0	-1.2		+1.2				
Receive Gain Tracking Error 3	$GT3_R$	A-law white noise input CCITT G. 712	-10 to -55dBm0		+0.1		dB			
			-55 to -60dBm0		+0.3					

(3) Frequency Response

Analog input operational amplifier gan = 1 (Non-inverting),
Receive output power amplifier gain = 1 Unbalanced
Output (PWRO+), unless otherwise specified.

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Transmit Channel Frequency Response	G_{RX} 1	Gain relative to gain at 1.02kHz, 0 dBm0	16.67Hz			-30	dB		
	G_{RX} 2		50Hz			-25			
	G_{RX} 3		60Hz			-23			
	G_{RX} 4		200Hz	-1.8		-0.125			
	G_{RX} 5		0.3 to 3.0kHz	-0.125		+0.125			
	G_{RX} 6		3.3kHz	-0.35		+0.03			
	G_{RX} 7		3.4kHz	-0.7		-0.1			
	G_{RX} 8		4.0kHz			-14			
	G_{RX} 9		4.6kHz and above			-32			
Receive Channel Frequency Response	G_{RR} 1	Gain relative to gain at 1.02kHz, 0 dBm0	Below 200Hz			+0.125	dB		
	G_{RR} 2		200Hz	-0.5		+0.125			
	G_{RR} 3		0.3 to 3.0kHz	-0.125		+0.125			
	G_{RR} 4		3.3kHz	-0.35		+0.03			
	G_{RR} 5		3.4kHz	-0.7		-0.1			
	G_{RR} 6		4.0kHZ			-14			
	G_{RR} 7		4.6kHz and above			-30			

(4) Noise

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Max.
Transmit Noise	$N_{XC}1$	AIN+ is grounded to AGND. Input amplifier gain = 1, C-Message filter is used.			15	dBrnc0	
	$N_{XC}2$	AIN+ is grounded to AGN. Input amplifier gain = 1, C-Message filter is used. Signaling data is added to the sixth frame.			18	dBrnc0	
	N_{XP}	AIN+ is grounded to AGND. Input amplifier gain = 1, Psophometric filter is used.			-75	dBm0p	
Receive Noise	$N_{RC}1$	C-Message filter is used. D_R = 11111111, measure at PWRO+			11	dBrnc0	
	$N_{RC}2$	C-Message filter is used. Input to D_R is zero code with sign bit toggled at 1kHz rate			12	dBrnc0	
	N_{RP}	Psophometric filter is used. D_R = lowest positive decode level			-79	dBm0p	
Single Frequency Noise	N_{SF}	End-to-End measurement CCITT G. 712 4.2			-50	dBm0	
Crosstalk, Transmit to Receive	CT_{TR}	D_R = lowest positive decode level AIN+ = 0 dBm0, 1.02kHz analog signal measure at PWRO+			-71	dB	
Crosstalk Receive to Transmit	CT_{RT}	AIN+ is grounded to AGND, DR = 0 dBm0, 1.02kHz digital signal			-71	dB	
Power Supply Rejection	$PSRR_T$ 1	+200mV P-P signal on V_{DD}, 0 to 50 kHz		40		dB	
	$PSRR_T$ 2	+200mV P-P signal on V_{SS}, 0 to 50kHz		40		dB	
	$PSRR_R$ 1	+200mV P-P signal on V_{DD}, 0 to 50kHz, PWRO+		30		dB	
	$PSRR_R$ 2	+200mV P-P signal on V_{SS}, 0 to 50kHz, PWRO+		30		dB	

(5) Distortion

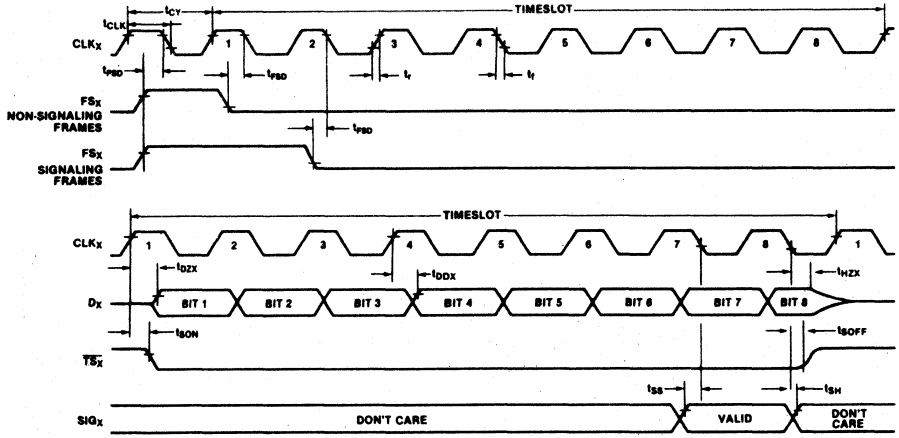
Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
Transmit Signal to Distortion	$SD1_X$	μ-law CCITT G. 712 Method 2	0 to -30 dBm0	36			dB			
			-40 dBm0	30						
			-45 dBm0	25						
	$SD2_X$	A-law CCITT G. 712 Method 2	0 to -30 dBm0	36			dB			
			-40 dBm0	30						
			-45 dBm0	25						
	$SD3_X$	A-law CCITT G. 712 Method 1	-6 to -27 dBm0		38		dB			
			-34 dBm0		36					
			-40 dBm0		31					
			-55 dBm0		16					
Receive Signal to Distortion	$SD1_R$	μ-law CCITT G. 712 Method 2	0 to -30 dBm0	36			dB			
			-40 dBm0	30						
			-45 dBm0	25						
	$SD2_R$	A-law CCITT G. 712 Method 2	0 to -30 dBm0	36			dB			
			-40 dBm0	30						
			-45 dBm0	25						
	$SD3_R$	A-law CCITT G. 712 Method 1	-6 to -27 dBm0		38		dB			
			-34 dBm0		36					
			-40 dBm0		31					
			-55 dBm0		16					
Transmit Single-Frequency Distortion Products	DP_X	AT&T Advisory No. 64 (3.8) 0 dBm0 input signal				-46	dBm0			
Receive Single-Frequency Distortion Products	DP_R	AT&T Advisory No. 64 (3.8) 0 dBm0 input signal				-46				

(5) Distortion cont'd.

Item	Symbol	Parameter/Conditions		Min.	Typ.	Max.	Unit	Customer Spec. Typ	Customer Spec. Max.
Inter-modulation Distortion	IMD1	End-to-End measurement CCITT G. 712 (7.1)				-35	dB		
	IMD_2	End-to-End measurement CCITT G. 712 (7.2)				-49	dBmO		
Spurious Out-of-band Signals	SOS	End-to-End measurement CCITT G. 712 (6.1)				-25	dBmO		
Spurious In-band Signals	SIS	End-to-End measurement CCITT G. 712 (9)				-40			
Transmit Absolute Delay	D_{AX}	Fixed Data Rate f_{CLKX} = 2.048MHz			245		μs		
Transmit Differential Envelope Delay	D_{DX}	Realtive to D_{AX}	500 to 600 Hz		170		μs		
			600 to 1000 Hz		95				
			1000 to 2600 Hz		45				
			2600 to 2800 Hz		105				
Receive Absolute Delay	D_{AR}	Fixed Data Rate f_{CLKR} = 2.048MHz			190		μs		
Receive Differential Envelope Delay	D_{DR}	Relative to D_{AR}	500 to 600 Hz		45		μs		
			600 to 1000 Hz		35				
			1000 to 2600 Hz		85				
			2600 to 2800 Hz		110				

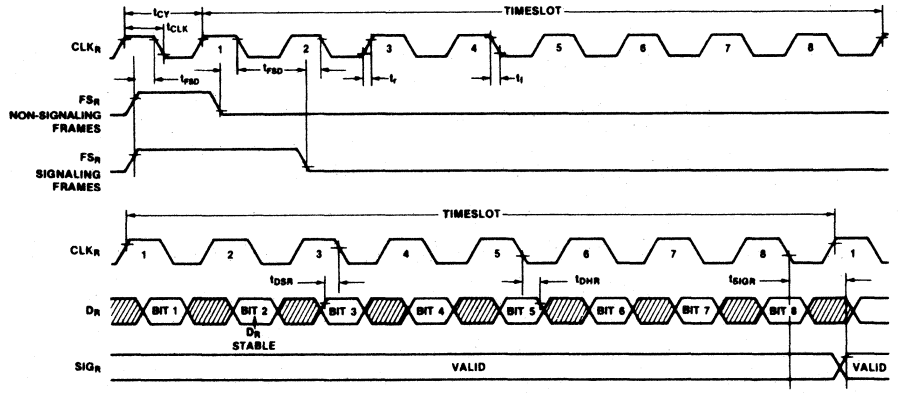
Waveforms
Fixed Data Rate Timing

TRANSMIT TIMING



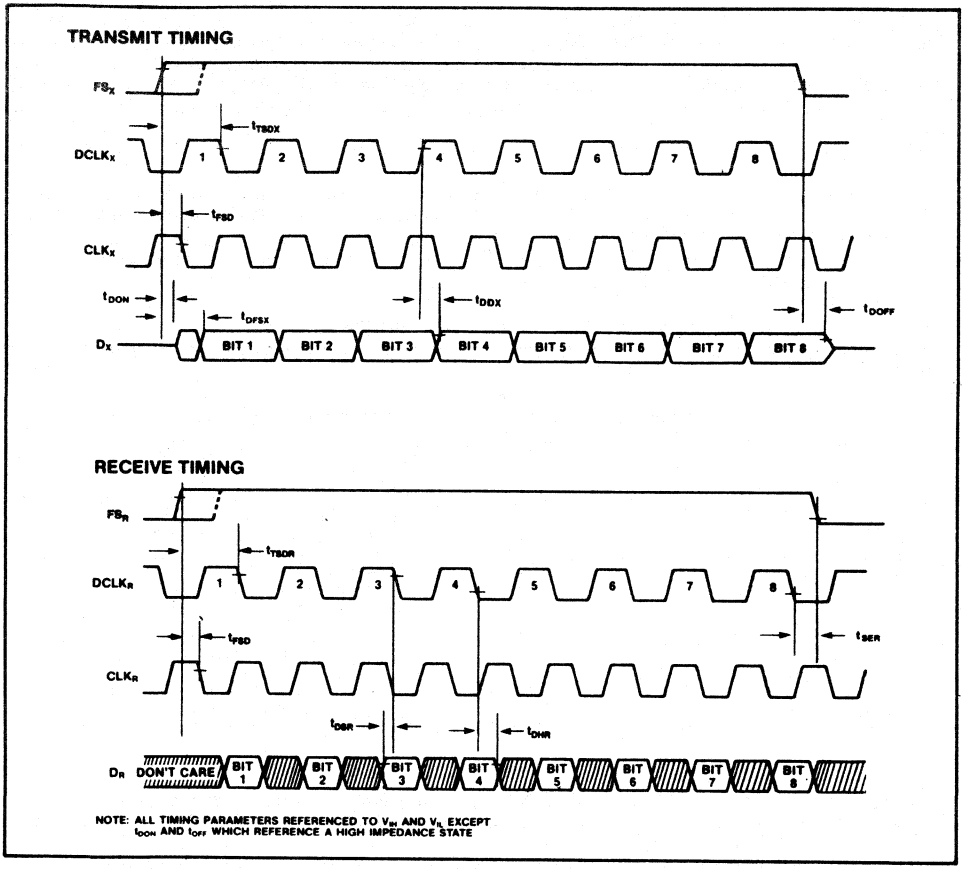
NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DZX}, t_{SOFF} AND t_{HZX} WHICH REFERENCE A HIGH IMPEDANCE STATE

RECEIVE TIMING

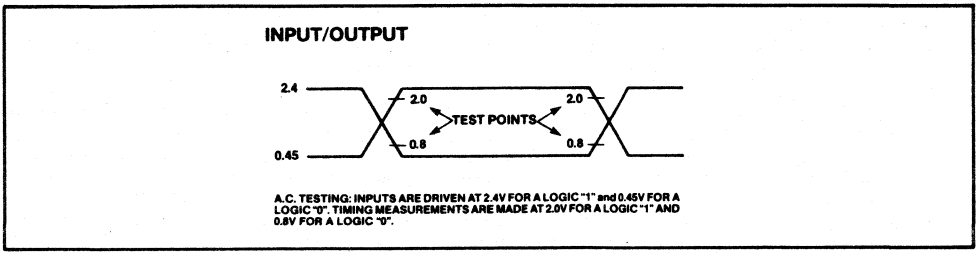


NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL}.

Variable Data Rate Timing



A.C. Testing Input, Output Waveform



General Operation

1. Functions Immediately After Power-Up

   The μPD9513D and 9514D have internal resets on power-up to protect other devices on the PCM highway during the power-up sequence. Therefore, certain delays for the start of functioning are provided on each digital output pin. Digital outputs D_X and $\overline{TS_X}$ are held in a high impedance state for four frames (500μs) after power is applied, and SIG_R is held low for four frames. The SIG_R pin will remain low unless a new setting by a signaling frame is made.

   Analog circuits such as filters, sample holds, and D/A converters require 60ms to begin functioning due to the autozero circuit.

2. Power-Down and Standby Modes

   * Power-Down Mode

   Power-down mode can be achieved by setting the $\overline{PDN}$ pin to low after which digital outputs D_X and $\overline{TS_X}$ will go to high within 10μs and the SIG_R pin will be set to low. In this mode, only the internal power-down controller, data clock, and frame sync buffers are enabled. Other circuits are disabled.

   Returning to power-up mode can be done by setting the $\overline{PDN}$ pin to high. The function begins after the same delay as in the power-up sequence.

   * Standby Mode

   The standby mode can be achieved by setting FS_X and/or FS_R to low level.

   The standby mode leaves the user an option of powering down either channel separately or powering down the entire device by selectively removing FS_X and/or FS_R.

Device	Power-Down Method	Typical Power Consumption	Digital Output Status
Power-Down Mode	$\overline{PDN}$ = TTL low	8 mW	$\overline{TS_X}$ and D_X are placed in a high impedance state and SIG_R is placed in a low level within 10μs after a low level signal is applied to PDN.
Standby Mode	FS_X and FS_R are TTL lowel	8 mW	$\overline{TS_X}$ and D_X are placed in a high impedance state and SIG_R is placed in a low level within 300 ms after FSX and FS_R are set to low.
Only transmit is on standby	FS_X is TTL low	40 mW	$\overline{TS_X}$ and D_X are placed in a high impedance state within 300ms after FS_X is set to low.
Only receive is on standby	FS_R is TTL low	40 mW	SIG_R is placed in a low impedance state within 300ms after FX_R is set low.

3. Fixed Data Rate Mode

   Fixed data rate mode is selected by connecting the $DCLK_R$ pin to the V_{SS} pin. In this mode, master clocks required to drive circuits, such as internal transmit/receive switched capacitor filters and D/A converters, are produced internally based on the data clocks supplied to CLK_X and CLK_R.

   Available data clock frequencies are 2.048, 1.544, or 1.536 MHz, and are selected by the CLKSEL pin. A singlewide frame-synchronization pulse designates a non-signaling frame, while a double-wide sync pulse enables the signaling function.

   In transmit section, if FS_X is high at the falling edge of the data clock applied to the CLK_X pin, the next rising edge of the data clock sets the D_X pin (tri-state output) to active, and a sign bit data (BIT 1) is output. In the same manner, each data for seven consecutive bits is clocked out at each of seven consecutive rising edges. Then the eighth falling edge of the data clock sets the D_X pin to a floating state.

   The $\overline{TS_X}$ remains at low level during the time the D_X pin is active.

   Similarly, on the receive side, if FS_R is high at the falling edge of the data clock applied to the CLK_R pin, data are latched by consecutive falling edges of the data clock and consecutively clocked in.

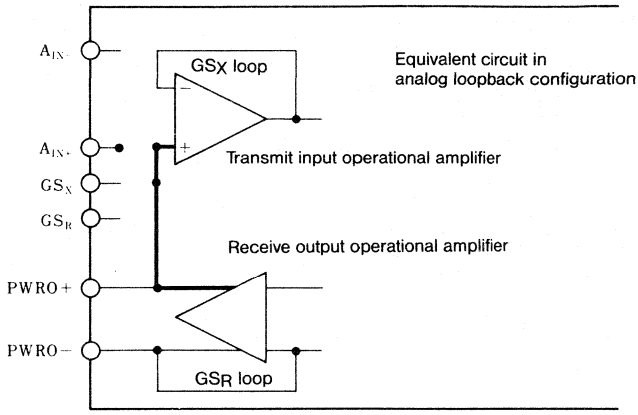
4. Variable Data Rate Mode

   Variable data rate mode is selected by inputting the receive data clock of TTL level (0 to V_{DD}) to the $DCLK_R$ pin rather than connecting the $DCLK_R$ pin to the V_{SS} pin.

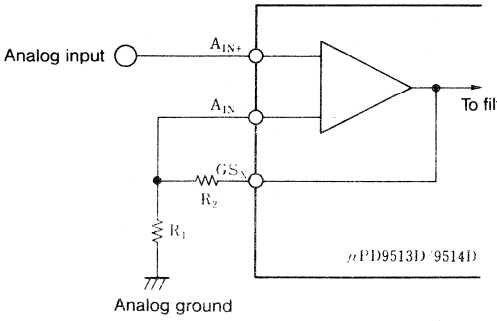
   This functional mode requires master clocks to drive such circuits as internal transmit/receive switched capacitor filters and D/A converters, data clock for data transfer, and frame synchronization clocks. Master clocks are applied to the CLK_R and CLK_X pins at frequencies of 2.048, 1.544, or 1.536 MHz, which can be selected by the CLKSEL pin.

   The data clocks are applied to the $DCLK_R$ and $DCLK_X$, at frequencies that can be varied from 64 kHz to 2.048 MHz. In this mode, the frame sync signal to FS_X and FS_R must be held high for one timeslot interval.

5. Signaling
The μPD9514D has a function that places/obtains signaling information to/from the PCM data stream. This function is available only in the fixed data rate mode. Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-wide frame sync pulse. On the transmit side, when signaling is specified, the signal present on SIG_X is substituted for the eighth bit (LSB) data of the PCM data to be transmitted, then output.
6. Bit steal
When signaling is specified on the receive side, the voice signal needs to be composed of bits because the LSB of the 8-bit PCM data is used for signaling. Even in this case, for the purpose of minimizing deterioration in SD and GT caracteristics, the composing side of the D/A converter is modified to compensate for the lost LSB data, assuming that half the overall data are lost.
7. Analog Loopback Test
The μPD9514D also has an internal analog loopback test function as a feature. When LOOP is set to high, PWRO+ is internally connected to AIN+, GS_R is internally connected to PWRO–, and AIN– is internally connected to GS_X. A 0dBm0 code sent into D_R will emerge from D_X as a + edBm0 digital signal. Thus, the maximum signal input level which can be tested using analog loopback is 0dBm0.



8. Gain Setting of Transmit Analog Input Operational Amplifier
On the transmit side, an analog input operational applifier is provided with inverting input, non-inverting input and output pins (AIN^+, AIN^-, and GS_X respectively), enabling various applications. For normal use as a non-inverting amplifier, gain settings of 0 to 20dB, load resistance (including gain setting resistance) of greater than 10 KΩ, and a load capacitance of less than 50pF should be used.

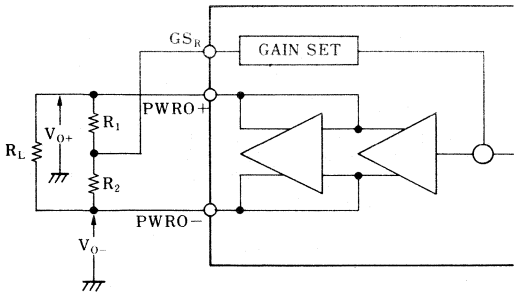


Gain $Av = 1 + \frac{R_2}{R_1}$

Load resistance $R_L = R_1 + R_2$

9. Gain Setting of Receive Analog Output Power Amplifier

The receive analog output power amplifier is capable of balanced or unbalanced output. In balanced output, a 600Ω load can be directly driven. In unbalanced output, a 300Ω load can be directly driven. Two resistors are used to set the gain within the range of 0 to −12dB.



Output voltage $V_O = (V_{O+}) - (V_{O-})$; total differential response

Gain $A_V = \dfrac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$

where,

$0.25 < Av < 1$,

$10\,K\Omega < R_1 + R_2 < 100\,K\Omega$

To set $A_V = 1$, connect the GS_R pin to the PWRO− pin.

To set $A_V = 0.25$, connect the GS_R pin to the PWRO+ pin.

μPD9516D/9517D
PCM COMBO

The μPD9516D and μPD9517D are single-chip PCM CODEC (COMBO) LSIs with transmit/receive filters. The μPD9516D is μ-law compatible, and the μPD9517D is A-law compatible. The data transmission mode, either fixed data rate or variable data rate, can be selected by pin connection.
In the variable data rate mode, data transfer can vary from 64kbps to 2.048Mbps. Therefore, this mode is especially suitable in digital telephone systems requiring low data transfer rates. The fixed data rate mode is suitable in standard 32-channel switching systems utilizing a 2.048MHz master clock.
These CODEC LSIs have wide dynamic ranges. Therefore, they can be used in various applications such as digital processing of voice signals, in addition to applications in communication systems.

Features

- These are complete single-chip PCM CODECs (COMBO), with the following circuits internally provided:
  - ○ Transmit channel input operational amplifier
  - ○ Transmit channel RC active LPF and switched capacitor HPF/LPF
  - ○ μ-law/A-law compatible coder and decoder
  - ○ Autozero circuit
  - ○ Receive channel switched-capacitor LPF
  - ○ Receive channel balanced output power amplifier
  - ○ High accuracy reference voltage circuit
  - ○ Serial I/O interface circuit
- μ-law compatible (μPD9516D)
  A-law compatible (μPD9517D)
- Two types of data transmission modes:
  Fixed data rate (2.048 Mbps)
  Variable data rate (64kbps to 2.048Mbps)
- Balanced/unbalanced output power amplifier capable of directly driving a 600Ω load is internally supported as a receive output amplifier
  80mW TYP. (normal operation)
  8mW TYP. (power-down mode)
- Single-chip CMOS monolithic LSI
- 16-pin ceramic DIP
- 9516AD/9517AD same specification as 9516D/9517D but latch up free

Note: Parameters exceeding the values specified in the following tables, should be filled-in by each customer in the specially reserved columns (Customer specification) and returned to NEC.
Additional information needed:

Date : _____

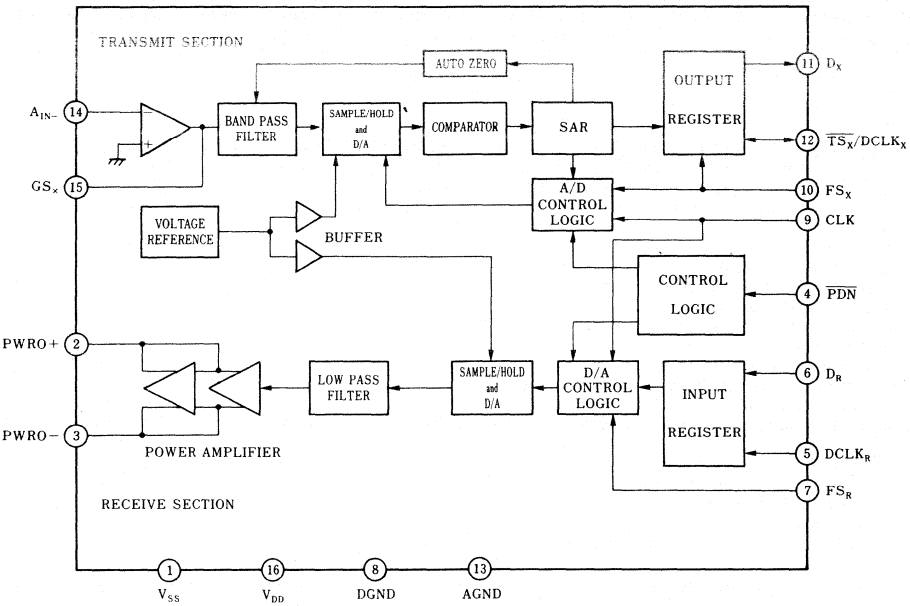
Customer Name : _____

Potential Quantity : _____

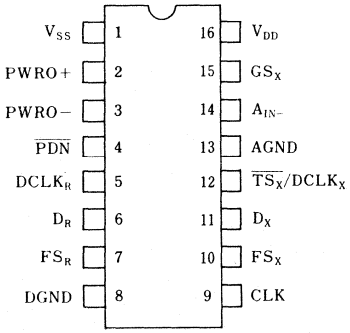
Project Timing : _____

Block Diagram

μPD9516D/μPD9517D

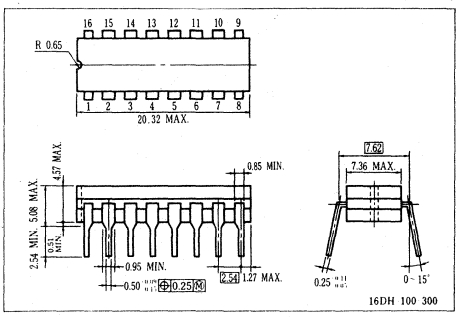


Pin Connections



Package Dimensions (Unit : mm)

16 pin ceramic DIP (300mil)



Pin Descriptions

Pin No. μPD9516D/9517D	Symbol	Input/ Output	Function
1	V_{SS}	– –	Negativ supply: input voltage is –5V ± 0.25V.
2	PWRO+	Output	Non-inverting output of receive power amplifier. Can directly drive 600Ω load (in a differential configuration).
3	PWRO–	Output	Inverting output of receive power amplifier. Functionally identical and complementary to PWRO+.
4	$\overline{PDN}$	Input	Power-down select (active low).
5	$DCLK_R$	Input	Selects fixed or variable data rate mode. ● When $DCLK_R$ is connected to V_{SS}, fixed data rate mode is selected. ● When $DCLK_R$ is not connected to V_{SS}, variable mode is in effect. In this mode, $DCLK_R$ becomes the receive data clock which operates at 64Kbps to 2.048Mbps.
6	D_R	Input	Receive PCM input. 8-bit PCM data are clocked in on this lead for eight consecutive falling edges of the receive data clock: CLK_R for fixed data rate mode, and $DCLK_R$ for variable data rate mode.
7	FS_R	Input	8kHz frame synchronization clock input, receive channel. ● In fixed data rate mode, distinguishes between signaling and nonsignaling frames by means of a double- or single-wide pulse, respectively. ● In variable data rate mode, this signal must remain high for the entire length of the timeslot. Receive channel enters the standby state whenever this pin is held low for 300ms.
8	DGND	– –	Digital ground. Not internally tied to analog ground.
9	CLK	Input	Transmit master clock pin. (2.048 MHz) Transmit master and data clock for the fixed data rate mode (in variable data rate mode, transmit master clock only).
10	FS_X	Input	8kHz frame synchronization clock input, transmit channel. ● In fixed data rate mode, distinguishes between signaling and nonsignaling frames by single- and double-wide pulses, respectively. ● In variable data mode, this signal must remain high for the entire length of the timeslot. Transmit channel enters the standby state whenever this pin is held low for 300ms.
11	D_X	Output	Transmit PCM output. 8-bit PCM data are clocked out on this lead for eight consecutive rising edges of the transmit data clock: CLK in fixed data rate mode, and $DCLK_X$ in variable data rate mode.

Pin No. μPD9516D/9517D	Symbol	Input/ Output	Function
12	$\overline{TSX}$/ DCLKX	Output/ Input	Transmit channel timeslot strobe output or data clock input for the transmit channel. ● In fixed data rate mode, this pin is an open drain output, and the transmit channel strobe signal is output. ● In variable data rate mode, this pin becomes the transmit data clock input pin which operates at 64kbps to 2.048Mbps.
13	AGND	– –	Analog ground pin. Not internally connected to digital ground.
14	AIN–	Input	Transmit inverting analog input pin.
15	GSX	– –	Transmit operational amplifier output pin. Internally connected to the filter of the next stage.
16	VDD	– –	Positive power supply: +5 ± 0.25V.

Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Parameter/ Conditions	Rating	Unit	Customer Spec. Rating
Supply Voltage	V_{DD}		−0.3 to +7.0	V	
	V_{SS}		−7.0 to +0.3		
Analog Input Voltage	V_{AIN}	AIN−, GSx	V_{SS} −0.3 to V_{DD} +0.3	V	
Digital Input Voltage	V_{DIN1}	For pins other than $DCLK_R$	−0.3 to V_{DD} +0.3	V	
	V_{DIN2}	$DCLK_R$ pins	V_{SS} −0.3 to V_{DD} +0.3		
Voltage Applied to Digital Output Pin	V_{DOUT}	For all digital output pins	−0.3 to V_{DD} +0.3	V	
Power Dissipation	P_T		500	mW	
Operating Temperature	T_{opt}		0 to +70	°C	
Storage Temperature	T_{stg}		−65 to +150	°C	
Soldering Temperature	T_{sold}	Less than 10 seconds	+260	°C	

Note: All voltages are based on the condition that $V_{DG} = V_{AG} = 0$, unless otherwise specified.
It should be connected to Analog ground with shorting at the just under position of IC between AGND and DGND pins.

Recommended Operating Conditions

V_{DD} = +5 ± 0.25V, V_{SS} = −5 ± 0.25V, $V_{DG} = V_{AG}$ = 0,
$0 \leqq T_a \leqq 70$°C, unless otherwise specified

(1) D.C. Conditions

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
Supply Voltage	V_{DD}			+4.75	+5.0	+5.25	V			
	V_{SS}			−5.25	−5.0	−4.75				
Load Resistance	R_{LAX}	Transmit amplifier		10			kΩ			
Load Capacitance	C_{LAX}					50	pF			
Load Resistance	R_{LAR}	Receive amplifier	Unbalanced output	300			Ω			
			Balanced output	600						
Load Capacitance	C_{LAR}		PWRO+, PWRO− pins			100	pF			
Input Low Voltage	V_{IL}	(See Note.)		0		0.8	V			
Input High Voltage	V_{IH}			2.0		V_{DD}				

Note: When $DCLK_R$ pin is connected to V_{SS} pin, the fixed data rate mode is selected.

(2) Clock

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
Master Clock Frequency	f_{CLK} ($1/t_{cy}$)			2.048		MHz			
Master Clock Duty Cycle	t_{CDC}		45	50	55	%			
Data Clock Frequency	f_{DCLK} ($1/t_{DCY}$)		64		2048	KHz			
Master Clock Pulse Width	t_{CLK}		220			ns			
Frame Sync Frequency	f_{FS}		7.9996	8.0000	8.0004	kHz			
D_R Setup Time	t_{DSR}		10			ns			
D_R Hold Time	t_{DHR}		60						
Frame Sync Delay Time	t_{FSD}		100		t_{CY}–100	ns			
Clock Rise Time	t_r				30	ns			
Clock Fall Time	t_f				30				

Timing In Variable Data Rate Mode

Item	Symbole	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Max.
Timeslot Delay	t_{TSD}	Referenced to $DCLK_X$ $DCLK_R$	140		t_{DCY}–140	ns		
Frame Sync Delay	t_{FSD}		100		t_{CY}–100	ns		
Data Clock Pulse Width	t_{DCW}		220			ns		
Time slot Hold Time	t_{TSH}		0			ns		

Note: $t_{DCY} = 1/f_{DCLK}$, $t_{CY} = 1/f_{CLK}$

64KB Operation, Variable Data Rate Mode

Item	Symbole	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Max.
Transmit Frame Sync Minimum Downtime	t_{FSLX}	FS_X is TTL high for remainder of frame	488			ns		
Receive Frame Sync Minimum Downtime	t_{FSLR}	FS_R is TTL high for remainder of frame	1952			ns		
Data Clock Pulse Width	t_{DCW}				10	μs		

D.C. Electrical Characteristics

$0 \leqq T_a \leqq 70°C$, $V_{DD} = +5 \pm 0.25V$, $V_{SS} = -5 \pm 0.25V$,
$V_{DG} = V_{AG} = 0$, $f_{DCLKR} = f_{DCLKX} = 2.048$ MHz
All outputs unloaded unless otherwise specified
Typical values are for $T_A = 25°C$, $V_{DD} = +5V$, and $V_{SS} = -5V$

(1) Power Dissipation

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Typ	Customer Spec. Max.
Operating Current	I_{DD}	In normal operation		8.0	13.0	mA		
	$\lvert I_{SS} \rvert$			8.0	13.0			
Power-Down Current	I_{DDPD}	$\overline{PND}$ pin is set to low after 10μs		0.8	1.3			
	$\lvert I_{SSPD} \rvert$			0.8	1.0			
Standby Current	I_{DDST}	FS_X and FS_R are set to low after 300ms		0.8	1.3			
	$\lvert I_{SSST} \rvert$			0.8	1.0			
Operating Power Dissipation	P_D	In normal operation		80	136.5	mW		
Power-Down Dissipation	P_{DPD}	$\overline{PDN}$ pin is set to low after 10μs		8	12.1			
Standby Power Dissipation	P_{DST}	FS_X and FS_R are set to low after 300 ms		8	12.1			

(2) Digital Interface

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Typ	Customer Spec. Max.
Digital Input Current	I_{ID1}	$0 \leqq V_{DIN} \leqq V_{DD}$			10	μA			
	I_{ID2}	$DCLK_R$ PINS $V_{SS} \leqq V_{DIN} \leqq V_{DD}$			10				
Output Low Voltage	V_{OL}	D_X, $\overline{TS_X}$, PINS $I_{OL} \leqq 3.2mA$			0.4	V			
Output High Voltage	V_{OH}	D_X pin ($I_{OH} \leqq 9.6mA$)	2.4						
Digital Output Capacitance	C_{OD}			5		pF			
Digital Input Capacitance	C_{ID}				10				

(3) Transmit Amplifier

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Input Leakage Current	I_B	$-2.17 \leqq V_{AIN} \leqq 2.17V$, AIN–,			100	nA		
Input Resistance	R_{IN}		10000			kΩ		
Input Offset Voltage	V_{IO}		–25		25	mV		
Voltage Gain	A_V		5000					

(4) Receive Power Amplifier

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ	Max.
Output Offset Voltage	V_{OS}	Unbalanced output connection, PWRO+ and PWRO– pins	–150	–75	150	mV			
Output Resistance	R_{ORR}	PWRO+, PWRO–		1		Ω			

A.C. Electrical Characteristics

$0 \leqq T_a \leqq 70°C$, $V_{DD} = 5 \pm 0.25$ V, $V_{SS} = -5 \pm 0.25$ V
$V_{DG} = V_{AG} = 0$,

(1) Timing Parameters in Fixed Data Rate Mode

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Max.
Data Enable Delay	t_{DZX}	CL < 100pF	0		145	ns		
Data Delay	t_{DDX}	CL < 100pF	0		145	ns		
Data Hold Time	t_{HZX}	CL = 0	60		220	ns		
$\overline{TSX}$ Enable Delay	t_{SON}	CL < 100pF	0		145	ns		
$\overline{TSX}$ Disable Delay	t_{SOFF}	CL = 0	50		210	ns		

(2) Timing Parameters in Variable Data Rate Mode

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Max.
DX Active Delay	t_{DON}	CL < 100pF	0		65	ns		
DX Inactive Delay	t_{DOFF}	CL < 100pF	0		90	ns		
Data Delay	t_{DFSX}		0		140	ns		
Data Delay	t_{DDX}	CL < 100pF	0		100	ns		

Transmission Characteristics

$T_a = 25°C$, $V_{DD} = 5 \pm 0.25V$, $V_{SS} = -5 \pm 0.25V$, $V_{AG} = V_{OG} = 0$
analog input signal level Vin = OdBm0 (f = 1020Hz),
analog input operational amplifier gain = 1 (inverting),
digital input signal level OdBm0 (f = 1020Hz),
unbalanced output (PWRO+), unless otherwise specified.

(1) Gain Characteristics

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Encoder Milliwatt Response (Transmit gain tolerance)	EmW	$V_{DD} = 5V$, $V_{SS} = -5V$	−0.15		+0.15	dBm0		
EmW Variation with Temp. and Power Supply	EmW_{TS}	$0 \leqq T_a \leqq 70°C$ $V_{DD} = 5 \pm 0.25V$ $V_{SS} = -5 \pm 0.25V$	−0.12		+0.12	dB		
Digital Milliwatt Response (Receive Gain Tolerance)	DmW	Measure relative to $OTLP_R$. Signal input per CCITT recommendation G.711. Output signal of 1000Hz. $V_{DD} = 5V$, $V_{SS} = -5V$	−0.15		+0.15	dBm0		
DmW Variation with Temp. and Power Supply	DmW_{TS}	$0 \leqq T_a \leqq 70°C$ $V_{DD} = 5 \pm 0.25V$ $V_{SS} = -5 \pm 0.25V$	−0.08		+0.08	dB		

Zero Transmission Level Points

Item	Symbol	Parameter/Conditions	Value	Unit	Customer Spec. Value
Zero Transmission Level Point Transmit Channel (μPD9516D)	$OTLP1_X$	Referenced to 600Ω	+2.76	dBm	
		Referenced to 900Ω	+1.00		
Zero Transmission Level Point Transmit Channel (μPD9517D)	$OTLP2_X$	Referenced to 600Ω	+2.79	dBm	
		Referenced to 900Ω	+1.03		
Zero Transmission Level Point Receive Channel (μPD9516D)	$OTLP1_R$	Referenced to 600Ω	+5.76	dBm	
		Referenced to 900Ω	+4.00		
Zero Transmission Level Point Receive Channel (μPD9517D)	$OTLP2_R$	Referenced to 600Ω	+5.79	dBm	
		Referenced to 900Ω	+4.03		

(2) Gain Tracking (Variation of gain with input level)
(Reference level = −10dBm0, unless otherwise specified)

(2)-1 μPD9516D

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Transmit Gain Tracking Error 1	$GT1_X$	CCITT G. 712 Method 2	+3 to −40dBm0	−0.25		+0.25	dB		
			−40 to −50dBm0	−0.5		+0.5			
			−50 to −55dBm0	−1.2		+1.2			
Receive Gain Tracking Error 1	$GT1_R$	CCITT G. 712 Method 2 $R_L = 300\Omega$ RWRO+	+3 to −40dBm0	−0.25		+0.25	dB		
			−40 to −50dBm0	−0.5		+0.5			
			−50 to −55dBm0	−1.2		+1.2			

(2)-2 μPD9517D

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Min.	Customer Spec. Typ	Customer Spec. Max.
Transmit Gain Tracking Error 2	$GT2_X$	CCITT G. 712 Method 2	+3 to −40dBm0	−0.25		+0.25	dB			
			−40 to −50dBm0	−0.5		+0.5				
			−50 to −55dBm0	−1.2		+1.2				
Transmit Gain Tracking Error 3	$GT3_X$	white noise input CCITT G. 712	−10 to −55dBm0		−0.1		dB			
			−55 to −60dBm0		−0.3					
Receive Gain Tracking Error 2	$GT2_R$	CCITT G. 712 Method 2 $R_L = 300\Omega$ RWRO+	+3 to −40dBm0	−0.25		+.0.25	dB			
			−40 to −50dBm0	−0.5		+0.5				
			−50 to −55dBm0	−1.2		+1.2				
Receive Gain Tracking Error 3	$GT3_R$	white noise input CCITT G. 712	−10 to −55dBm0		+0.1		dB			
			−55 to −60dBm0		+0.3					

(3) Frequency Response

Analog input operational amplifier gain = 1 (inveriting)
Unbalanced output (PWRO+)
unless otherwise specified.

								Customer Spec.	
Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Min.	Max.
Transmit Channel Frequency Response	G_{RX} 1	Gain relative to gain at 1.02kHz, 0 dBm0	16.67Hz			-30	dB		
	G_{RX} 2		50Hz			-25			
	G_{RX} 3		60Hz			-23			
	G_{RX} 4		200Hz	-1.8		-0.125			
	G_{RX} 5		0.3 to 3.0kHz	-0.125		+0.125			
	G_{RX} 6		3.3kHz	-0.35		+0.03			
	G_{RX} 7		3.4kHz	-0.7		-0.1			
	G_{RX} 8		4.0kHz			-14			
	G_{RX} 9		4.6kHz and above			-32			
Receive Channel Frequency Response	G_{RR} 1	Gain relative to gain at 1.02kHz, 0 dBm0	Below 200Hz			+0.125	dB		
	G_{RR} 2		200Hz	-0.5		+0.125			
	G_{RR} 3		0.3 to 3.0kHz	-0.125		+0.125			
	G_{RR} 4		3.3kHz	-0.35		+0.03			
	G_{RR} 5		3.4kHz	-0.7		-0.1			
	G_{RR} 6		4.0kHZ			-14			
	G_{RR} 7		4.6kHz and above			-30			

(4) Noise

(4)-1 μPD9516D, μPD9517D

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Typ	Customer Spec. Max.
Single Frequency Noise	N_{SF}	End-to-End measurement CCITT G. 712 4.2			-50	dBm0		
Crosstalk, Transmit to Receive	CT_{TR}	D_R = lowest positive decode level V_{AIN} = 0 dBm0 1.02 KHz analog signal, measure at PWRO+			-71	dB		
Crosstalk Receive to Transmit	CT_{RT}	V_{AIN} is grounded to AGND, D_R = 0 dBm0 1.02kHz digital signal			-71	dB		
Power Supply Rejection	$PSRR_{T1}$	+200mV P-P signal on V_{DD}, 0 to 50kHz		40		dB		
	$PSRR_{T2}$	+200mV P-P signal on V_{SS}, 0 to 50kHz		40		dB		
	$PSRR_{R1}$	+200mV P-P signal on V_{DD}, 0 to 50kHz PWRO+		30		dB		
	$PSRR_{R2}$	+200mV P-P signal on V_{SS}, 0 to 50kHz, PWRO+		30		dB		

(4)-2 μPD9516D

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Max.
Transmit Noise	N_{XC} 1	V_{AIN} is grounded to AGND. Input amplifier gain = 1, C-Message filter is used.			15	dBrnc0	
Receive Noise	N_{RC} 1	C-Message filter is used. D_R = 11111111, measure at PWRO+			11	dBrnc0	
	N_{RC} 2	C-Message filter is used. Input to D_R is zero code with sign bit toggled at 1kHz rate			12	dBrnc0	

(4)-3 μPD9517D

Item	Symbol	Parameter/Conditions	Min.	TYP.	Max.	Unit	Customer Spec. Max.
Transmit Noise	N_{XP}	V_{AIN} is grounded to to AGND. Input amplifier gain = 1, Psophometric filter is used.			-75	dBm0p	
Receive Noise	N_{RP}	Psophometric filter is used. D_R = lowest positive decode level			-79	dBm0p	

(5) Distortion

(5)-1 μPD9516D, μPD9517D

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Typ	Customer Spec. Max.
Transmit Single-Frequency Distortion Products	DP_X	AT&T Advisory No. 64 (3.8) 0 dBm0 input signal (μPD9516D)				-46	dBm0		
Receive Single-Frequency Disortion Products	DP_R	AT&T Advisory No. 64 (3.8) 0 dBm0 input signal (μPD9516D)				-46			
Inter-modulation Distortion	IMD_1	End-to-End measurement CCITT G. 712 (7.1)				-35	dB		
	IMD_2	End-to-End measurement CCITT G. 712 (7.2)				-49	dBm0		
Spurious Out-of-band Signals	SOS	End-to-End measurement CCITT G. 712 (6.1)				-25	dBm0		
Suprious In-band Signals	SIS	End-to-End measurement CCITT G. 712 (9)				-40			
Transmit Absolute Delay	D_{AX}	Fixed Data Rate F_{CLK} = 2.048MHz			245		μs		
Transmit Differential Envelope Delay	D_{DX}	Relative to D_{AX}	500 to 600Hz		170		μs		
			600 to 1000Hz		95				
			1000 to 2600Hz		45				
			2600 to 2800Hz		105				
Receive Absolute Delay	D_{AR}	Fixed Data Rate f_{CLK} = 2.048MHz PWRO+			190		μs		
Receive Differential Envelope Delay	D_{DR}	Relative to D_{AR}	500 to 600Hz		45		μs		
			600 to 1000Hz		35				
			1000 to 2600Hz		85				
			2600 to 2800HZ		110				

(5)-2 μPD9516D

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Min.
Transmit Signal to Distortion	$SD1_X$	CCITT G. 712 Method 2	0 to -30dBm0	36			dB	
			-40dBm0	30				
			-45dBm0	25				
Receive Signal to Distortion	$SD1_R$	CCITT G.712 Method 2	0 to -30dBm0	36			dB	
			-40dBm0	30				
			-45dBm0	25				

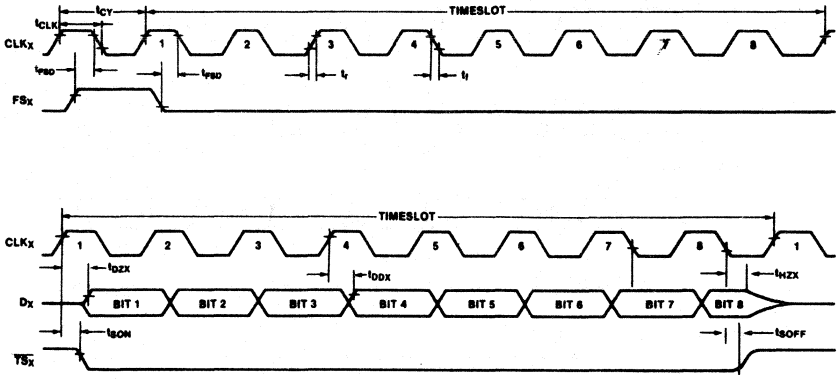
(5)-3 μPD9517D

Item	Symbol	Parameter/Conditions		Min.	TYP.	Max.	Unit	Customer Spec. Min.	Typ
Transmit Signal to Distortion	$SD2_X$	CCITT G. 712 Method 2	0 to -30dBm0	36			dB		
			-40dBm0	30					
			-45dBm0	25					
	$SD3_X$	CCITT G. 712 Method 1	-6 to -27dBm0		38		dB		
			-34dBm0		36				
			-40dBm0		31				
			-55dBm0		16				
Receive Signal to Distortion	$SD2_R$	CCITT G. 712 Method 2	0 to -30dBm0	36			dB		
			-40dBm0	30					
			-45dBm0	25					
	$SD3_R$	CCITT G. 712 Method 1	-6 to -27dBm0		38		dB		
			-34dBm0		36				
			-40dBm0		31				
			-55dBm0		16				

WAVEFORMS

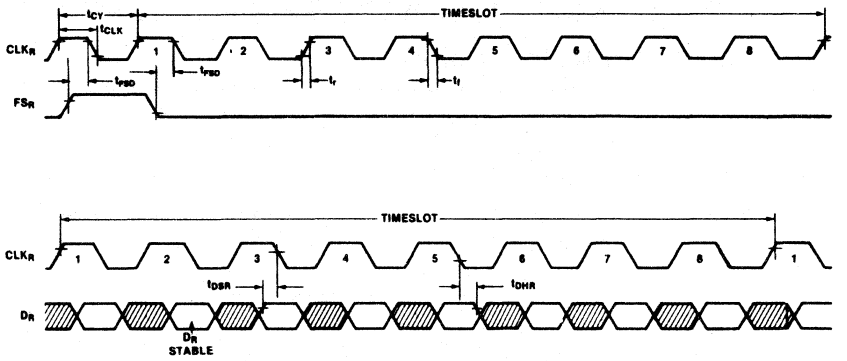
Fixed Data Rate Timing

TRANSMIT TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DZX}, t_{SOFF} AND t_{HZX} WHICH REFERENCE A HIGH IMPEDANCE STATE

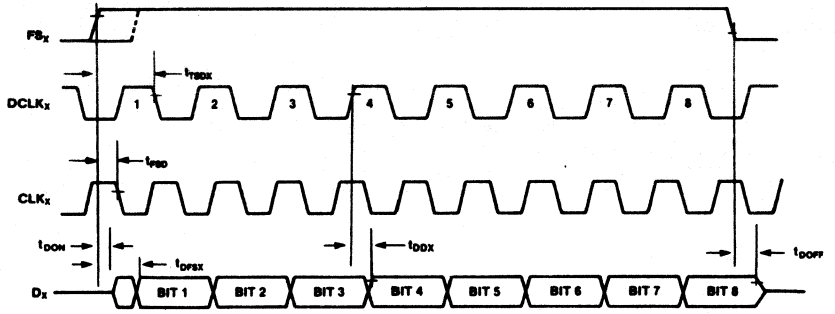
RECEIVE TIMING



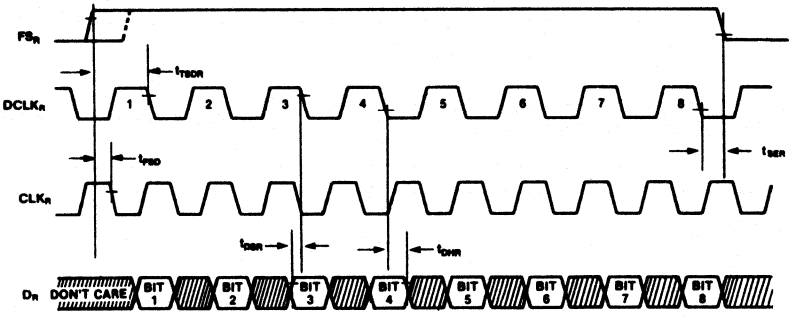
NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL}.

VARIABLE DATA RATE TIMING

TRANSMIT TIMING



RECEIVE TIMING



NOTE: ALL TIMING PARAMETERS REFERENCED TO V_{IH} AND V_{IL} EXCEPT t_{DON} AND t_{OFF} WHICH REFERENCE A HIGH IMPEDANCE STATE

A.C. TESTING INPUT, OUTPUT WAVEFORM

INPUT/OUTPUT

A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" and 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

General Operation

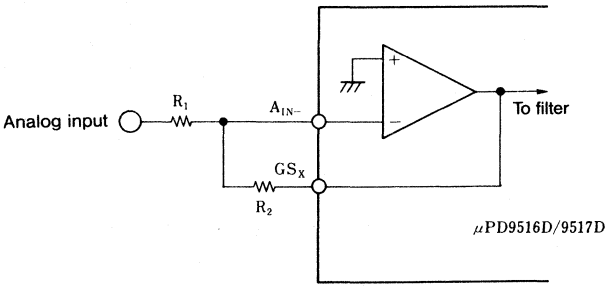
1. Functions Immediately After Power-Up
   The μPD9516D and 9517D have internal resets on power-up to protect other devices on the PCM highway during the power-up sequence. Therefore, certain delays for the start of functioning are provided on each digital output pin. Digital outputs D_X and $\overline{TS_X}$ are held in a high impedance state for four frames (500μs) after power is applied.
   Analog circuits such as filters, sample holds, and D/A converters require 60ms to begin functioning due to the autozero circuit.
2. Power-Down and Standby Modes
   * Power-Down Mode
   Power-down mode can be achieved by setting the $\overline{PDN}$ pin to low after which digital outputs D_X and $\overline{TS_X}$ will go to high within 10μs impedance. In this mode, only the internal power-down controller, data clock, and frame sync buffers are enabled. Other circuits are disabled.
   Returning to power-up mode can be done by setting the $\overline{PDN}$ pin to high. The function begins after the same delay as in the power-up sequence.
   * Standby Mode
   The standby mode can be achieved by setting FS_X and/or FS_R to low level.
   The standby mode leaves the user an option of powering down either channel separately or powering down the entire device by selectively removing FS_X and/or FS_R.

Device	Power-Down Method	Typical Power Consumption	Digital Output Status
Power-Down Mode	$\overline{PDN}$ = low level	8 mW	$\overline{TS_X}$ and D_X are placed in a high impedance state within 10μs after a low level signal is applied to PDN.
Standby Mode	FS_X and FS_R are low level	8 mW	$\overline{TS_X}$ and D_X are placed in a high impedance state within 300ms after FS_X and FS_R are set to low.
Only transmit is on standby	FS_X is low	40 mW	$\overline{TS_X}$ and D_X are placed in a high impedance state within 300ms after FS_X is set to low.
Only receive is on standby	FS_R is low	40 mW	

3. Fixed Data Rate Mode
Fixed data rate mode is selected by connecting the $DCLK_R$ pin to the V_{SS} pin. In this mode, master clocks required to drive circuits, such as internal transmit/receive switched capacitor filters and D/A converters, are produced internally based on the data clocks supplied to CLK_X and CLK.
The data clock frequency is 2.048MHz. In transmit section, if FS_X is high at the falling edge of the data clock applied to the CLK pin, the next rising edge of the data clock sets the D_X pin (tri-state output) to active, and a sign bit data (BIT 1) is output. In the same manner, each data for seven consecutive bits is clocked out at each of seven consecutive rising edges. Then the eighth falling edge of the data clock sets the D_X pin to a floating state.
The $\overline{TS_X}$ remains at low level during the time the D_X pin is active.
Similarly, on the receive side, if FS_R is high at the falling edge of the data clock applied to the CLK pin, data are latched by consecutive falling edges of the data clock and consecutively clocked in.

4. Variable Data Rate Mode
Variable data rate mode is selected by inputting the receive data clock of TTL level (0 to V_{DD}) to the $DCLK_R$ pin rather than connecting the $DCLK_R$ pin to the V_{SS} pin.
This functional mode requires master clocks to drive such circuits as internal transmit/receive switched capacitor filters and D/A converters, data clock for data transfer, and frame synchronization clocks. Master clocks are applied to the CLK pins at a frequency of 2.048MHz.
The data clocks are applied to the $DCLK_R$ and $DCLK_X$, at frequencies that can be varied from 64kHz to 2.048Mhz. In this mode, the frame sync signal to FS_X and FS_R must be held high for one timeslot interval.

5. Gain Setting of Transmit Analog Input Operational Amplifier
On the transmit side, an analog input operational amplifier is provided with inverting input and output pins (AIN^- and GS_X respectively), enabling various applications. Gain settings of 0 to 20dB, load resistance (including gain setting resistance) of greater than 10Ω and a load capacitance of less than 50pF should be used.



Gain $Av = -\frac{R_2}{R_1}$

Load resistance $R_L = R_2$

μPD9513/4/6/7D PCM COMBO

LATCH-UP CONSIDERATIONS

μPD951X Latch-up considerations

1. Latch-UP Protection for input/output pins.
   The characteristic of latch-up:
   For all input pins – over +/–20 mA at applied voltage +/–5V.
   For I/O and output pins – over +/–50 mA at +/–0.5V.
   In spite of protection circuitry, combo's have still latch-up problems in power-up sequence. It is a destiny for CMOS devices.

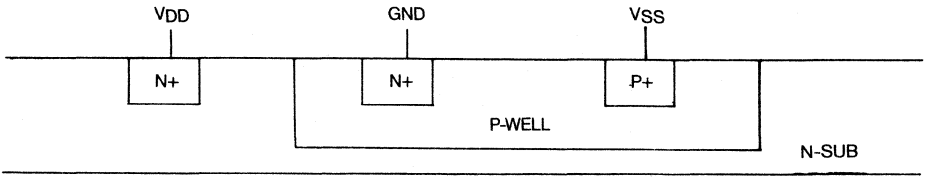
2. Latch-up Protection for Power Up Sequence
   The μPD951X family are LSI in CMOS technology which have four power supply pins, I. E. V_{DD}, V_{SS}, AGND and DGND. Therefore, latch-up will occur based on the power-up sequence.
   In case of μPD951X, the sequences are the following four. Please note that in the followings no additional shottky diodes are required.
   1. V_{DD} – V_{SS} – A + DGND
   2. V_{SS} – V_{DD} – A + DGND
   3. A + DGND – V_{SS} – V_{DD}
   4. V_{SS} – A + DGND – V_{DD}

   Note: AGND pin and DGND pin should be connected to each other very closely to the device, then to the external analog GND/line on PCB.
   When the customer keeps the above sequences, we guarantee that the latch-up problem will not occur within the absolute max. ratings.

3. Recommendations
   - Only a small change from a existing NMOS COMBO line card (PCB) are required to avoid CMOS COMBO Latch-up at power-up sequence.
     i.e. – Connecting A GND and D GND close to 951x package on PCB.
     – Four power sequences are available.
   - By using CMOS COMBO's instead of NMOS ones, following advantages are offered:
     – Better Reliability
     – Lower Power Dissipation
     – Lower Power-Down Current
     – Better PSRR
     – Better Transmission Characteristics

4. APPENDIX 1
   Latch-up mechanism
   A) Latch-up mechanism by power-up sequence
      – in case of 1) A + DGND to V_{DD} to V_{SS} and 2) V_{DD} to A + DGND to V_{SS}

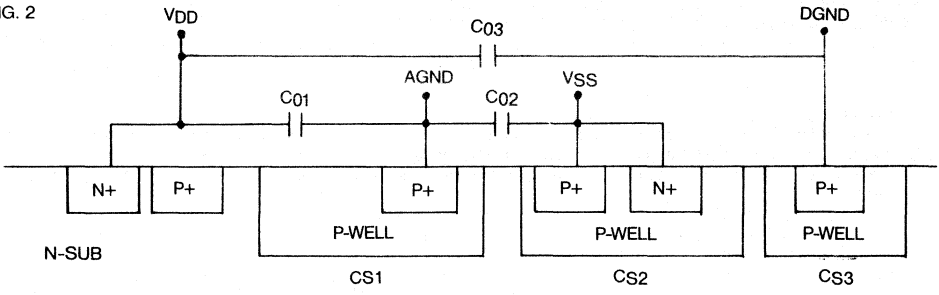
FIG. 1



When a potential of the GND and V_{DD} are clamped, the P-Well which has V_{SS} potential will go to the V_{DD} potential due to coupling capacitance between P-Well and N-Sub.
However N+ which is already clampled to GND potential, is existing. Therefore a diode which consists of the P-Well and the N+ will be biased as forward direction.
As a result, many electrons will be injected to the N-Sub from the N+ connected to the GND. Those electrons will cause a latch-up.

B) The reason why AGND and DGND should be connected to each other very closely to the outside device.
In actual application, by-pass capacitors should be connected between V_{DD} pin and GND pins respectively between V_{SS} pin and GND pin as follows:

FIG. 2



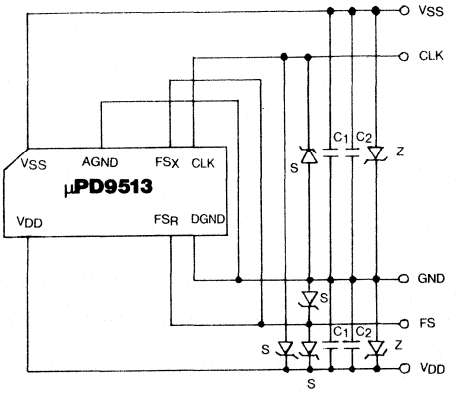
If AGND and DGND are not connected to each other, latch-up will occur, even if the power-up sequence is V_{SS}-DGND-AGND-V_{DD}. The reason is as follows:
When V_{SS} and DGND are connected to power supply, potential of V_{DD} and AGND are floating. Therefore potential of V_{DD} will be charged up to a certain voltage which is specified by by-pass capacitors C_{01}, C_{02} and C_{03}. (If $C_{01} = C_{02} = C_{03}$, its voltage is around $1/3V_{SS}$.)
A diode which consists of DGND's P-Well and floating N-Sub (V_{DD}), will be applied around 1/3 V_{SS} as forward direction. Then many holes will be injected to the N-Sub from DGND's P+. As a result, latch-up may occur.

C) In case of power-up after connection of AGND and DGND
In this case, when V_{SS}, AGND and DGND are connected to power supply, a potential of AGND is low impedance, and a capacitance between V_{SS} and V_{DD} is only coupling capacitance C_{S2}.
Therefore a potential of V_{DD} that is floating will be almost same as that of GND which will be divided by $C = C_{01} // C_{03}$ and C_{S2}. Thus AGND and DGND's P-Well and N-Sub have almost same potential as GND, so that no hole will be injected. As a result no latch-up will occur.

Conclusion:
The AGND and DGND should be shorted and connected to an external analog GND potential.

APPENDIX 2
Protection Circuit for life-test and burn-in testing.

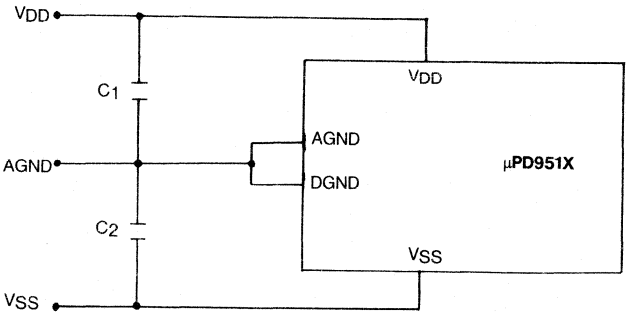
So far the BT circuit is concerned, we recommend to use following circuit. Protection diodes and capacitors are connected to avoid latch-up during burn-in testing.



$C_1 = 22\,\mu F$ $C_2 = 0{,}1\,\mu F$
Z ; Zenner (12V) S ; Schottkey

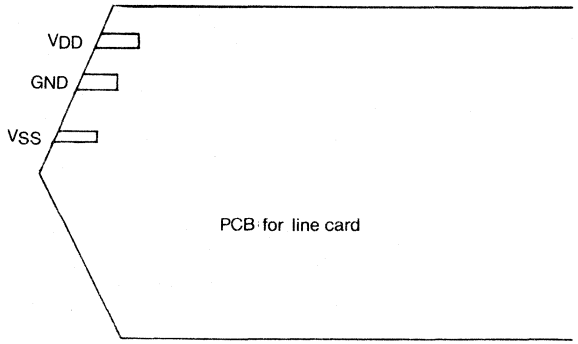
We deliberately have to exclude th probability of latch-up with this BT circuit, because Burn-In Testing is measuring the reliability performance of the device itself. So, we have to guard devices against unexpecting noise on power rail and clock input caused by furnaces.

APPENDIX 3
Recommended protection circuit for a line card



Note that no diode is required for protection.

Following tapering PCB are also recommended for appropriate power-up sequence.



μPD9601D/9602D
PCM COMBO

The μPD9601D and μPD9602D are single-chip PCM CODEC (COMBO) LSIs with transmit/receive filters. These CODEC LSIs have PLL circuits for transmit and receive channels, that can generate a clock for internal circuit by the frame synchronization clock. The μPD9601D is A-law compatible, and the μPD9602D is μ-law compatible.

FEATURES:

- There are complete single-chip PCM CODECs (COMBO), with the following circuits internally provided:
  - ○ Transmit channel input operational amplifier
  - ○ Transmit channel RC active LPF and switched-capacitor HPF/LPF
  - ○ μ-law/A-law compatible coder and decoder
  - ○ Auto-zero circuit
  - ○ Receive channel switched-capacitor LPF
  - ○ Receive channel unbalanced output power amplifier (600 Ω load resistance)
  - ○ High accuracy reference voltage circuit
  - ○ Serial I/O interface circuit
  - ○ PLL circuits to generate transmit and receive internal clock
- A-law compatible (μPD9601D)
- μ-law compatible (μPD9602D)
- Capable of synchronous or asynchronous operation
- Data rate (64 Kbps to 2,048 Kbps)
- Low power dissipation
  - 50 mW TYP. (normal operation)
  - 5 mW TYP. (power-down mode or standby mode)
- Single-chip CMOS monolithic LSI
- 16-pin ceramic DIP

Note: Parameters exceeding the values specified in the following tables, should be filled-in by each customer in the specially reserved columns (Customer specification) and returned to NEC.
Additional information needed:

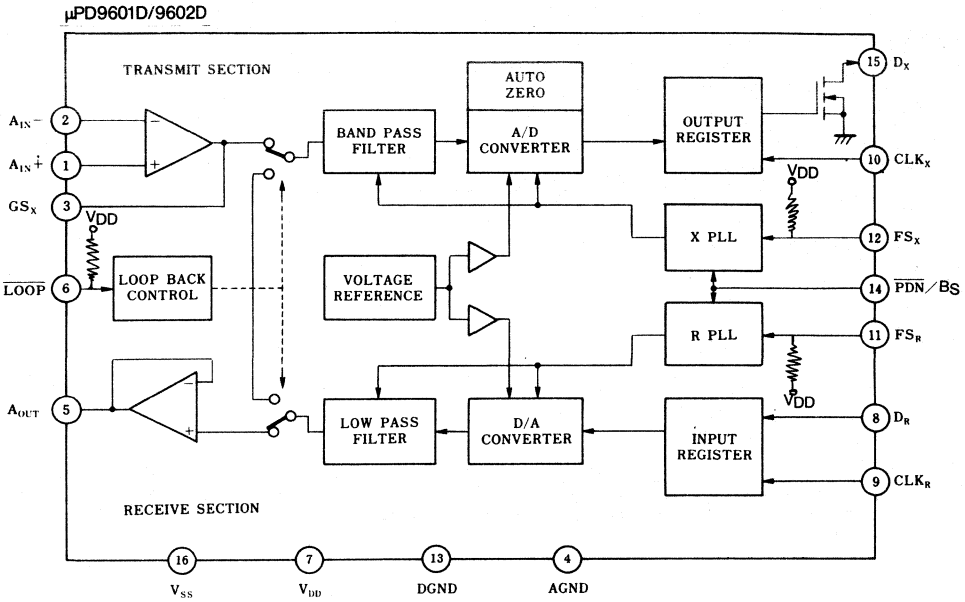
Date : _____

Customer Name : _____

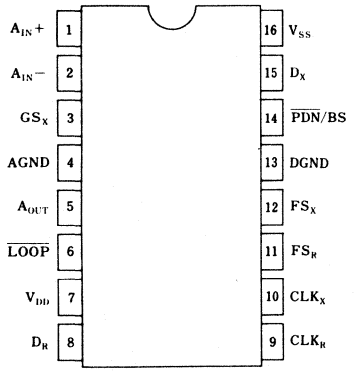
Potential Quantity : _____

Project Timing : _____

Block Diagram



Pin Connection (Top View)



PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Function
1	$A_{IN}+$	Input	Transmit operational amplifier noninverting analog input
2	$A_{IN}-$	Input	Transmit operational amplifier inverting analog input
3	GS_X	Output	Transmit operational amplifier output
4	AGND	– –	Analog ground, not internally connected to digital ground
5	A_{OUT}	Output	Receive power amplifier output
6*	$\overline{LOOP}$	Input (TTL level)	Input for analog loop back test control. This pin is left open or connected to V_{SS} (–5V) to prevent analog loop back test.
7	V_{DD}	– –	Positive power supply +5±0,25V
8	D_R	Input (TTL level)	Receive PCM input
9	CLK_R	Input (TTL level)	Receive channel data clock input. Clock frequency can be used from 64 KHz to 2,048 KHz. For CLK_X, either synchronous or asynchronous operation can be used, however for FS_R, only synchronous operation can be used.
10	CLK_X	Input (TTL level)	Transmit channel data clock input. Clock frequency can be used from 64 KHz to 2,048 KHz. For CLK_R, either synchronous or asynchronous can be used, however for FS_X, only synchronous operation can be used.
11*	FS_R	Input (TTL level)	Receive cannel frame synchronous clock input
12*	FS_X	Input (TTL level)	Transmit channel frame synchronous clock input
13	DGND	– –	Digital ground pin, not internally connected to analog ground
14	$\overline{PDN}$/BS	Input (TTL level)	Power-down/bit steal control input – in case of μPD9601: Both transmit/receive channel come to power-down mode by low level. – in case of μPD9602: Both transmit/receive channel come to power-down mode, when low level is kept over 7 frames (125μs x 7 = 875 μs). When H to L or L to H is done within 6 frames, bit steal will be achieved.
15	D_X	Output open drain	Transmit PCM data output
16	V_{SS}	– –	Negative power supply –5±0.25V

*Note: internally pulled up

Absolute Maximum Ratings ($T_a = 25°$)

Item	Symbol	Condition	Rating	Unit	Customer Spec. Rating
Supply Voltage	V_{DD}		−0.3 to +7.0	V	
	V_{SS}		−7.0 to +0.3		
Analog Input Voltage	V_{AIN}	$A_{IN}+$, $A_{IN}-$, GS_X	V_{SS}−0.3 to V_{DD}+0.3	V	
Digital Input Voltage	V_{DIN}		−0.3 to V_{DD}+0.3	V	
Voltage applied to Digital-output pin	V_{DOUT}	D_X pins	−0.3 to V_{DD}+0.3	V	
Power Dissipation	P_T		500	mW	
Operating Temp.	T_{opt}		0 to +70	°C	
Storage Temp.	T_{stg}		−65 to +150	°C	
Soldering Temp.	T_{sold}	< 10 sec.	260	°C	

Note: All voltages are based on the condition that VDG = VAG = 0, unless otherwise specified.

Recommended Operating Conditions

V_{DD} = +5±0.25V, V_{SS} = −5±0.25V, V_{DG} = V_{AG} = 0
0 ≦ T_a ≦ 70 C, unless otherwise specified.

(1) D.C. Conditions

Item	Symbol	Conditions		Min.	Typ	Max.	Unit	Customer Spec. Min.	Typ	Max.
Supply Voltage	V_{DD}			4.75	5.00	5.25	V			
	V_{SS}			−5.25	−5.00	−4.75				
Input Analog Voltage	V_{AX}	transmit amp.	A_{IN}+ pin	−3.0		3.0	V			
Gain Setting Range	GR_{AX}			0		15	dB			
Load Resistance	R_{LAX}		GS_X, A_{IN}- (note 2)	10			KΩ			
Load Capacitance	C_{LAX}					100	pF			
Load Resistance	R_{LAR}	receive amp.		600			Ω			
Load Capacitance	C_{LAR}					100	pF			
Input Low Voltage	V_{IL}			0		0.8	V			
Input High Voltage	V_{IH}			2.0		V_{DD}	V			

(2) A.C. Conditions

V_{DD} = 5±0.25V, V_{SS} = −5±0.25V, V_{DG} = V_{AG} = 0, (note 1)
0 ≦ T_a ≦ 70°C, unless otherwise specified.

Item	Symbol	Conditions	Min.	Typ	Max.	Unit	Customer Spec. Min.	Typ	Max.
Data Clock Frequency	f_{CLK}	(=1/t_{CY})	64		2048	kHz			
Data Clock width	t_{CLK}		200			ns			

(cont'd)

(2) A.C. Conditions (cont'd)

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Typ	Max.
Frame Synchronous Clock Frequency	f_S			8		kHz			
High-Level Frame Synchronous Clock width	t_{WFS}		200			ns			
Low-Level Frame Synchronous Clock width	t_{WLFS}		8			μs			
Clock Risetime	t_r				50	ns			
Clock Falltime	t_f				50	ns			
Synchronous timing margin 1	t_{CSD1}				100	ns			
Synchronous timing margin 2	t_{CSD2}		40			ns			
Frame Synchronous Clock and Data Clock High-Level Overlapping Width	t_{WHSC}		100			ns			
D_R Setup Time	t_{DSR}	note 3	65			ns			
D_R Hold Time	t_{DHR}	note 3	120			ns			
BS Setup Time	t_{BSR}	note 3	200			ns			
BS Hold Time	t_{BHR}	note 3	200			ns			

Note 1.: AGND pin and DGND pin should be connected each other close to the device's analog ground pin.
Note 2.: GSX pin and A_{IN}- pin should be connected each other, when an input gain is zero dB.
Note 3.: A rise/fall time of digital input signal and clock signal which are used at timing test, is around 5 ns.

D.C. Electrical Characteristics

$0° \leq T_a \leq 70°C$, $V_{DD} = 5 \pm 0.25V$, $V_{SS} = -5 \pm 0.25V$,
$V_{DG} = V_{AG} = 0$, $f_{CLKR} = f_{CLKX} = 2048$ kHz
All outputs unloaded unless otherwise specified.

(1) Power Dissipations

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Operating Current	I_{DD}	In normal operation		5	10.0	mA		
	$\lvert I_{SS} \rvert$			5	10.0			
Power-Down Current	I_{DDPD1}	$\overline{PDN}$ pin is set to low after 100 ms			1.0			
	$\lvert I_{SSPD1} \rvert$				0.2			
Standby Current	I_{DDPD2}	FS_X and FS_R are set to low after 100 ms			1.0			
	$\lvert I_{SSPD2} \rvert$				0.2			

(2) Digital Interface

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Digital Input Current	I_{ID}	$0 \leq V_{DIN} \leq V_{DD}$ $\overline{PDN}$/BS, D_R, CLK_X, CLK_R pins	−10		10	μA		
Pulled up Current	$\lvert I_{IL} \rvert$	$V_{DIN} = 0$ V FS_X, FS_R, $\overline{LOOP}$ pins		4	100			
Digital Output Leak Current	I_L	D_X pin $0 \leq V_{DIN} \leq V_{DD}$	−10		10			
Output Low Voltage	V_{OL}	D_X pin, $R_L = 500\Omega$ $I_{OL} = 0.8$mA			0.4	V		
Output High Voltage	V_{OH}	D_X pin, $I_{OL} \leq 150\mu A$	$V_{DD}-0.3$					
Digital Output Capacitance	C_{OD}	f = 1 MHz			15	pF		
Digital Input Capacitance	C_{ID}	f = 1 MHz			10			

(3) Transmit Amplifier

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Input Leakage Current	I_B	$-3.0 \leq V_{AIN} \leq 3.0$V $A_{IN}+$, $A_{IN}-$ pins	−10		10	μA		
Input Resistance	R_{IN}	f = 1 MHz	50			kΩ		
Input Offset Voltage	V_{IO}	$A_{IN}+$ pin	−500		500	mV		
Output Offset Voltage	V_{OG}	GS_X pin, $R_L = 10$ kΩ	−50		50	mV		
Max. Output Voltage	V_{OM}	GS_X pin, $R_L = 10$ kΩ	−3.0		3.0	V		
Input Capacitance	C_{AIN}				10	pF		

(4) Receive Power Amplifier

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Output Offest Voltage	V_{OA}	AOUT pin, D_R = +0 code	−50		50	mV		
Max. Output Voltage	V_{OM}	$R_L \geqq 600\Omega$	−2.5		2.5	V		
Output Resistance	R_{ORR}			1				

A.C. Electrical Characteristics

$0 \leqq T_a \leqq 70°C$, $V_{DD} = 5 \pm 0.25V$, $V_{SS} = -5 \pm 0.25V$, $V_{DG} = V_{AG} = 0V$,
$f_{CLKR} = f_{CLKX} = 2048$ kHz, $R_L = 500\ \Omega$, $C_L = 165$ pF,
$I_{OL} = 0.8$ mA, $I_{OH} \leqq 150\ \mu A$, unless otherwise specified.

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Data Enable Time 1	t_{DZX1}	DX pin (from FSX to DX)			170	ns		
Data Enable Time 2	t_{DZX2}	DXpin (from CLKX to DX)			120	ns		
Data Delay Time	t_{DDX}	DX pin			180	ns		
Data Hold Time	t_{HZX}	DX pin		50		ns		

Transmission Characteristics

1. μPD9601D

$T_a = 25°C$, $V_{DD} = 5 \pm 0.25$ V, $V_{SS} = -5 \pm 0.25$V, analog input signal level $V_{in} = 0$ dBm0 (f = 820 Hz), analog input gain = 0 dB, $V_{DG} = V_{AG} = 0$V, digital input signal level = 0 dBm0 (f = 820 Hz) unless otherwise specified.

(1) Zero Transmission Level Point

Item	Symbol	Condition	Min.	Typ	Max	Unit	Customer Spec. Min.	Typ	Max.
Zero Transmission Level Point (Transmit)	OPLX	$V_{DD}=5V$, $V_{SS}=-5V$		4.02		dBm			
Zero Transmission Level Point (Receive)	OTPLR			4.02		dBm			

(2) Gain Characteristics

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Typ	Max.
Transmit Gain Tolerance	GX	referenced 0TLPx, $V_{DD}=5V$	−0.1		0.1	dB			
Receive Gain Tolerance	GR	referenced 0TLPR, $V_{SS}=-5V$	−0.1		0.1	dB			
GX variation with Temp. & power supply	ΔGX	$0 \leqq T_a \leqq 70°C$	−0.2		0.2	dB			
GR variation with Temp. & power supply	ΔGR		−0.2		0.2	dB			

(3) Gain Tracking (Variation of gain with input level)

Item	Symbol	Condition		Min.	Typ	Max.	Unit	Customer Spec. Min.	Typ	Max.
Transmit Gain Tracking Error	GTX	CCITT G714 Method 2	+3 to −40dBm0	−0.2		+0.2	dB			
			−50	−0.4		+0.4				
			−55	−0.8		+0.8				
		CCITT G714 Method 1	−10 to −40dBm0		0.0		dB			
			−50		0.0					
			−55		0.0					
Receive Gain Tracking Error	GTR	CCITT G714 Method 2	+3 to −40dBm0	−0.2		+0.2	dB			
			−50	−0.4		+0.4				
			−55	−0.8		+0.8				
		CCITT G714 Method 1	−10 to −40dBm0		0.0		dB			
			−50		0.0					
			−55		0.0					

(3) Frequency Response

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Transmit Channel Frequency Response (Gain)	G_{RX1}	60 Hz			−24	dB		
	G_{RX2}	200 Hz	−2.5		+0.15			
	G_{RX3}	0.3 to 3 kHz	−0.2		+0.15			
	G_{RX4}	3.2 kHz	−0.65		+0.15			
	G_{RX5}	3.4 kHz	−0.8		+0.15			
	G_{RX6}	3.78 kHz			−6.5			
Receive Channel Frequency Response (Gain)	G_{RR1}	0 to 3.0 kHz	−0.2		+0.15	dB		
	G_{RR2}	3.2 kHz	−0.65		+0.15			
	G_{RR3}	3.4 kHz	−0.8		+0.15			
	G_{RR4}	3.78 kHz			−6.5			

(4) Noise

Item	Symbol	Condition		Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Transmit Noise	N_{XP}	$A_{IN}+$ is grounded to AGND. Input gain = 0 dB, use Psophometric filter	Min.		−72	dBm0p		
Receive Noise	N_{RP}	Use Psophometric filter, D_R = +0 code			−78			
Single Frequency Noise	N_{SF}	End-to-end testing CCITT G.712 4.2			−50	dBm0		
Crosstalk Transmit to Receive	CT_{TR}	D_R = lowest positive decode level, $A_{IN}+$ = 0 dBm0, 820Hz			−65	dB		
Crosstalk Receive to Transmit	CT_{RT}	$A_{IN}+$ is grounded to AGND. D_R = 0 dBm0, 820Hz digital input			−65			
Power Supply Rejection	$PSRR_1$	± 100mVop signal on V_{DD} or V_{SS}, f = 1kHz	30			dB		
	$PSRR_2$	± 100mVop signal on V_{DD} or V_{SS}, f = 3 kHz	20			dB		
	$PSRR_3$	± 100mVop signal on V_{DD} or V_{SS}, f = 3.4kHz	20			dB		

(5) Distortion

Item	Symbol	Condition		Min.	Typ	Max.	Unit	Customer Spec. Min.	Typ	Max.
Transmit Signal to Distortion	SD_X	CCITT G.714 Method 2	0 to −30 dBm0	36			dB			
			−40	31						
			−45	26						
		CCITT G.714 Method 1	−6 to −27		37		dB			
			−34		35					
			−40		30					
			−55		15					
Receive Signal to Distortion	SD_R	CCITT G.714 Method 2	0 to −30 dBm0	36			dB			
			−40	31						
			−45	26						
		CCITT G.714 Method 1	−6 to −27		37		dB			
			−34		35					
			−40		30					
			−55		15					
Inter-modulation Distortion	IMD_1	End-to-end measurement CCITT G.712 (7.1)				−38	dB			
	IMD_2	End-to-end measurement CCITT G.712 (7.2)				−52	dBm0			
Absolute Delay	D_A	A_{IN} to A_{OUT}				540	μs			
Group. Delay	D_O	A_{IN} to A_{OUT}	500 Hz			1.50	ms			
			600 Hz			0.75				
			1000 Hz			0.25				
			2600 Hz			0.25				
			2800 Hz			1.50				

Transmission Characteristics

2. μPD9602D

$T_a = 25°C$, $V_{DD} = 5 \pm 0.25$ V, $V_{SS} = -5 \pm 0.25$V, analog input signal level $V_{in} = 0$ dBm0 (F = 1020 Hz), analog input gain = 0 dB, $V_{DG} = V_{AG} = 0$V, digital input signal level = 0 dBm0 (F = 1020 Hz) unless otherwise specified.

(1) Gain Characteristics

Item	Symbol	Condition		Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Typ	Customer Spec. Max.
Zero Transmission Level Point (Transmit)	$0TLP_X$		$V_{DD} = 5V$		3.99		dBm			
Zero Transmission Level Point (Receive)	$0TLP_R$		$V_{SS} = -5V$		3.99		dBm			
Transmit Gain Tolerance	G_X	referenced $0TLP_X$		−0.1		0.1	dB			
Receive Gain Tolerance	G_R	referenced $0TLP_R$		−0.1		0.1	dB			
G_X variation with Temp. & power supply	dG_X	$0 \leqq T_a \leqq 70°C$		−0.15		0.15	dB			
G_R variation with Temp. & power supply	dG_R			−0.15		0.15	dB			

(2) Gain Tracking (Variation of gain with input level)

Item		Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Transmit Gain Tracking Error	GT_X	+3 to −40 dBm0	−0.2		+0.2	dB		
		−50	−0.4		+0.4			
		−55	−0.8		+0.8			
Receive Gain Tracking Error	GT_R	+3 to −40 dBm0	−0.2		+0.2	dB		
		−50	−0.4		+0.4			
		−55	−0.8		+0.8			

Zero Transmission Level Point

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Zero Transmission Level Point (Transmit)	$OTLP_X$	$V_{DD} = 5V$		3.99		dBm		
Zero Transmission Level Point (Receive)	$OTLP_R$	$V_{SS} = -5V$		3.99		dBm		

(3) Frequency Response

Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Transmit Channel Frequency Response (Gain)	G_{RX1}	60 Hz			−24	dB		
	G_{RX2}	200 Hz	−2.5		+0.15			
	G_{RX3}	0.3 to 3 kHz	−0.2		+0.15			
	G_{RX4}	3.2 kHz	−0.65		+0.15			
	G_{RX5}	3.4 kHz	−0.8		+0.15			
	G_{RX6}	3.78 kHz			−6.5			
Receive Channel Frequency Response (Gain)	G_{RR1}	0 to 3.0 kHz	−0.2		+0.15	dB		
	G_{RR2}	3.2 kHz	−0.65		+0.15			
	G_{RR3}	3.4 kHz	−0.8		+0.15			
	G_{RR4}	3.78 kHz			−6.5			

(4) Noise

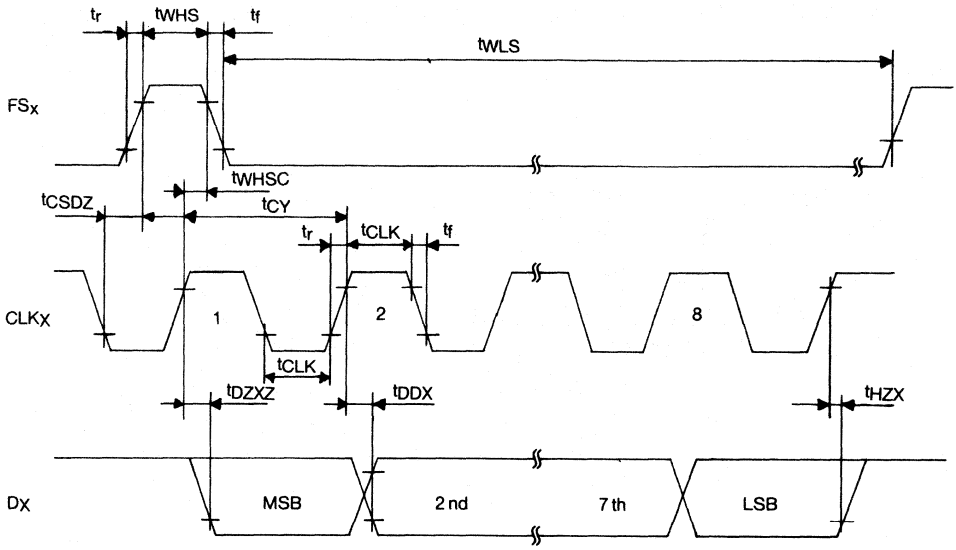
Item	Symbol	Condition	Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Transmit Noise	N_{XC}	$A_{IN}+$ is grounded to AGND. Input gain = 1, use C message filter			17	dBrnc0		
Receive Noise	N_{RC}	Use C message filter, D_R = +0 code			12			
Single Frequency Noise	N_{SF}	End-to-end testing CCITT G.712 4.2			−50	dBm0		
Crosstalk Transmit to Receive	CT_{TR}	D_R = lowest positive decode level, $A_{IN}+$ = 0 dBm0, 1020Hz			−65	dB		
Crosstalk Receive to Transmit	CT_{RT}	$A_{IN}+$ is grounded to AGND. D_R = 0 dBm0, 1020Hz digital input			−65			
Power Supply Rejection	$PSRR_1$	± 100mV$_{OP}$ signal on V_{DD} or V_{SS}, f=1kHz	30			dB		
	$PSRR_2$	± 100mV$_{OP}$ signal on V_{DD} or V_{SS}, f=3kHz	20			dB		
	$PSRR_3$	± 100mV$_{OP}$ signal on V_{DD} or V_{SS}, f=3.4kHz	20			dB		

(5) Distortion

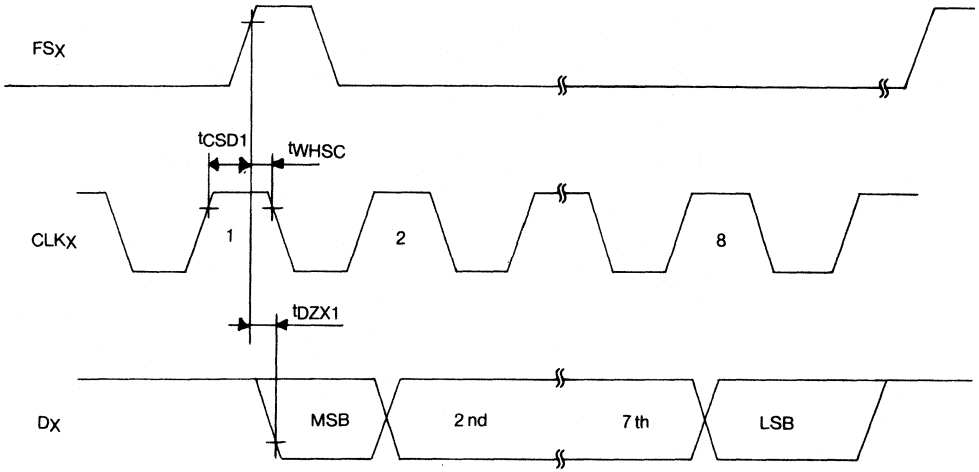
Item	Symbol	Condition		Min.	Typ	Max.	Unit	Customer Spec. Min.	Customer Spec. Max.
Transmit Signal to Distortion	SD_X	CCITT G.714 Methode 2	0 to −30 dBm0	36			dB		
			−40	31					
			−45	26					
Receive Signal to Distortion	SD_R	CCITT G.714 Method 2	0 to −30 dBm0	36			dB		
			−40	31					
			−45	26					
Inter-modulation Distortion	IMD_1	End-to-end measurement CCITT G.712 (7.1)				−38	dB		
	IMD_2	End-to-end measurement CCITT G.712 (7.2)				−52	dBm0		
Absolute Delay	D_A	A_{IN} to A_{OUT}				540	μs		
Group Delay	D_O	A_{IN} to A_{OUT}	500 kHz			1.50	ms		
			600 kHz			0.75			
			1000 kHz			0.25			
			2600 kHz			0.25			
			2800 kHz			1.50			

Timing Charts

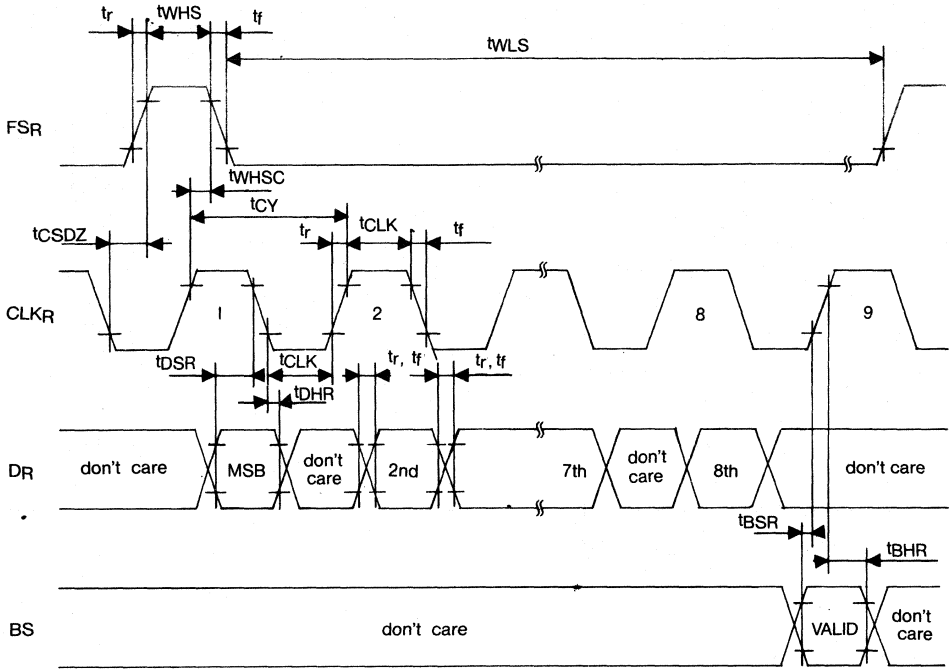
Transmit Timing (1)



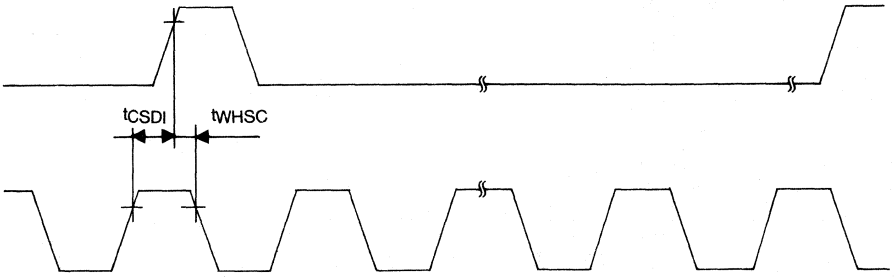
Transmit Timing (2)



Receive Timing (1)



Receive Timing (2)



General Operation

1. Functions Immediately After Power-Up

The μPD9601D and 9602D have internal power on reset circuits to protect other devices on the PCM highway during the power-up sequence.

Therefore, certain delays for the start of functioning are provided on both digital output pin and analog output pin. Digital output D_X is held in a high impedance state for around 5 ms after power is applied.

Analog circuits such as filters, sample helds, and D/A convertors requires 15ms to begin funtioning due to the settling time of analog circuits.

2. Power-Down and Standby Mode

- Power down mode:

  Power down mode can be achieved by setting the PDN/BS pin to TTL low level after which digital output D_X will go to high impedance state. In this mode, only the PLL circuits the internal power-down controller, data clock, and frame sync buffers are enabled. Other circuits are disabled.

  Returning to power-up mode can be done by setting the PDN/BS pin to TTL high level high. The function begins after the same delay as in the power-up sequence (without the lock-in time of PLL$_S$).

- Standby Mode

  The stanby mode can be achieved by setting FS_X and/or FS_R to TTL low level or open. The standby mode leaves the user an option of power down either channel separately or powering down the entire device by selectively removing FS_X and/or FS_R.

3. PCM Data Transmission

In transmit section, if FS_X is high at the falling edge of the data clock applied to the CLK_X pin, the next rising edge of the data clock sets the D_X pin to active, and a sign bit data (MSB) is output.

In the same manner, each data for seven consecutive bits is clocked out at each of seven consecutive rising edges. Then the ninth rising edge of the data clock sets the D_X pin to a high impedance state.

Similarly, on the receive side, if the FS_R is high at the falling edge of the data clock applied to the CLK_R pin, data are latched by consecutive falling edges of the data clock and consecutive clocked in.

4. Bit Steal

The μPD9602D has a decorder function of signaling frame including signaling information. When signaling is specified on the receive side, the voice signal needs to be composed of bits because the LSB of the 8-bit PCM data is used for signaling. Even in this case, for the purpose of minimizing deterioration in SD and GT characteristics, the composing side of the D/A converter is modified to compensate for the lost LSB data, assuming that half the overall data are lost. Also μPD9602D will be output 7-bit decoded signal by inputting alternated per each signaling frame to the PDN/BS pin. In this case, the LSB datas are ignored. However when over 7 frame of lowlevel is input to the PDN/BS pin, the device goes to a power-down mode.

5. Analog Loopback Test

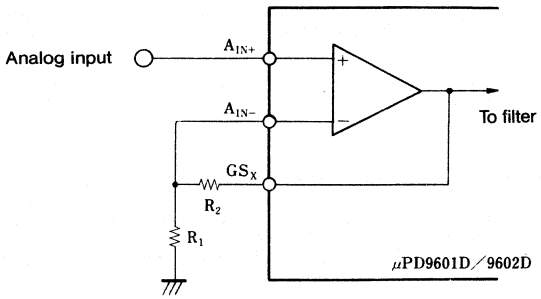
The μPD9601D and 9602D also have an analog loopback test function on chip as a feature. When LOOP bar pin is set to TTL low level, the LPF output of receive channel is internally connected to the BPF input of transmit channel. A 0 dBm0 digital tone signal sent to DR will emerge from D_X as a 0 dBm0 signal.

When not using this test function, the LOOP bar pin should be left open or connected to the V_{SS}. The LOOP bar is pulled up.

6. Gain Setting of Transmit Analog Input Operational Amplifier

On the transmit side, an analog input operational amplifier is provided with inverting input, non-inverting input and output pins (AIN+, AIN−, and GS_X respectively), enabling various applications.

For normal use as a non-inverting amplifier, gain settings of 0 to 15 dB, load resistance (including gain setting resistance) more than 10 kΩ, and a load capacitance of less than 100pF should be used.



Gain $A_V = 1 + \frac{R_2}{R_2}$

Load resistance $R_L = R_1 + R_2$

7. Operating Recommendations

a. Layout of AGND and DGND

It should be connected to Analog ground with shorting at the just under position of IC between AGND and DGND pins.

b. Power-up sequence

The μPD9601 D and μPD9602D two powering pins and two ground pins. The recommended power-up sequence is:

I V_{SS} − AGND − DGND − V_{DD}
II V_{DD} − V_{SS} − A, DGND
III V_{SS} − V_{DD} − A, DGND
IV V_{SS}A, DGND − V_{DD}
V V_{SS} − A, DGND − V_{DD}

μPD9601/9602D
HITACH type COMBO's Lineup
VERSION B

		NEC	HITACHI			
Comp. Law	A	μPD9601D	HD44231	HD44233	HD44235	HD44237
	μ	μPD9602D	HD44232	HD44234	HD44236	HD44238
	5	Aout	Aout	Aout	Aout	Aout
	6	Loop	Vref	Vref	Vref	Vref
	Pin 8	DR	n.c.	DR	n.c.	DR
	No. 9	ClkR	DR	ClkR	DR	ClkR
	10	ClkX	Clk	ClkX	Clk	ClkX
	11	FSR	FS	FSR	FS	FSR
	12	FSX	n.c.	FSX	n.c.	FSX
Clock	Int. Clk.	PLL	COUNTER on chip		PLL on chip	
	PCM Clk. rate	variable 64 - 2048kHz	fixed data clock 1536/1544/2048 kHz		variable data clock 64-2048 kHz	
	SYNC/ ASYNC	BOTH	SYNC only	BOTH	SYNC only	BOTH
Output AMP	Type	SINGLE ENDED				
	Min. Load	600 ohm	1.2 Kohm		1,2 Kohm	
Others		Loop back test				
Compatibility		–	No	Yes	No	Yes

Note: If external reference voltage is not used, the Vref pin should be connected to V_{SS} pin or left open.
The same applies to $\overline{LOOP}$ pin of μPD9601D/9602D(external reference voltage cannot be used).

μPD9601D/D9602D/D9604D/D9605D

Hitachi based CMOS COMBOs Lineup

Version B

	Hitachi				NEC			
	44233	44234	44237	44238	D9601	D9602	D9604	D9605
Encoding Law	A	μ	A	μ	A	μ	μ	A
Interbal Clock	Divider		PLL		PLL			
PCM Data Rate	1.536Mbps Fixed 1.544Mbps 2.048 Mbps		Variable 64k~2.048Mbps		Variable 64k~2.048Mbps			
Analog Loopback Test	No Capability				Capable $\overline{LOOP}$ pin = TTL low level			
Voltage Reference	Internal: V_{REF} pin = Open or V_{SS} (−5V) External: V_{REF} pin = 2~3V				Internal only $\overline{LOOP}$ pin = Open or V_{SS} (−5V)			
Input Amplifier	Operational Amplifier with 2nd Order RC filter				Uncommitted Operational Amplifier			
Output Amplifier	Load Reisitance 3 Kohm		1.2 Kohm		Load Resistance 600 ohm			
Digital Gain Set	No Capability				No Capability		Capable 0~15.5 dB 0.5dB step	
Power Consumption	60mW(typ)		50mW (typ)		50mW (typ)			
Absolute Delay	540μsec (max)				540μsec (max)			
Gain Variation	±0.15dB (Temp. and power supply)				±0.2dB (Initial and Temp. and power supply)			
Bit Steal Control		No		Yes		Yes	Yes	
Note on Compatibility					Hitachi Compatible		NEC Original	

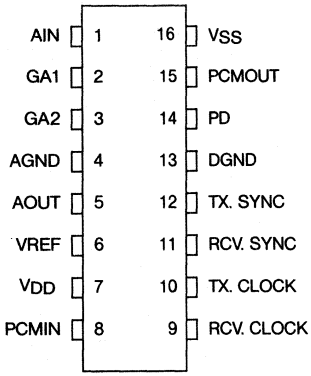
μPD9601AD/9602AD
HITACHI type COMBO's Lineup
VERSION C

		NEC	HITACHI				
Comp. Law	A	μPD9601AD	HD44231	HD44233	HD44235	HD44237	HD44247
	μ	μPD9602AD	HD44232	HD44234	HD44236	HD44238	HD44248
	5	Aout	Aout	Aout	Aout	Aout	Aout+
	6	Loop	Vref	Vref	Vref	Vref	Aout–
	Pin 8	DR	n.c.	DR	n.c.	DR	DR
	No. 9	ClkR	DR	ClkR	DR	ClkR	ClkR
	10	ClkX	Clk	ClkX	Clk	ClkX	ClkX
	11	FSR	FS	FSR	FS	FSR	FSR
	12	FSX	n.c.	FSX	n.c.	FSX	FSX
Clock	Int. Clk.	PLL	COUNTER on chip		PLL on chip		
	PCM Clk. rate	variable 64 - 2048kHz	fixed data clock 1536/1544/2048 kHz		variable data clock 64-2048 kHz		
	SYNC/ ASYNC	BOTH	SYNC only	BOTH	SYNC only	BOTH	BOTH
Output AMP	Type	SINGLE ENDED					PUSH-PULL
	Min. Load	600 ohm	600 ohm				600 ohm
Others		Loop back test					
Compatibility		–	No	Yes	No	Yes	No

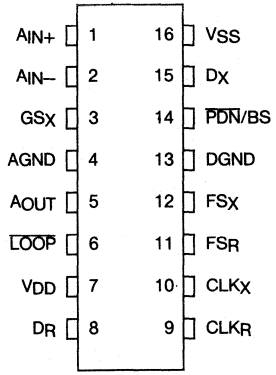
Note: If external reference voltage is not used, the Vref pin should be connected to V_{SS} pin or left open.
The same applies to $\overline{LOOP}$ pin of μPD9601D/9602D (external reference voltage cannot be used).

PACKAGE PIN CONFIGURATIONS

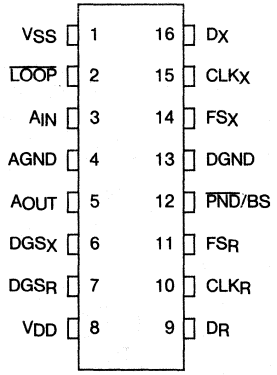
HD44233/234
HD44237/238



μPD9601/9602



μPD9604/9605



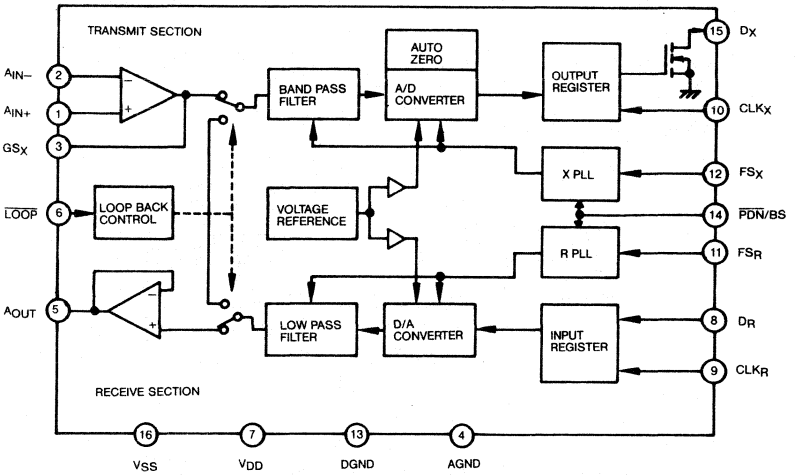
PIN NAMES SUMMARY TABLE

No	Hitachi	NEC	No	Hitachi	NEC
1	AIN	AIN+	9	RCV. CLOCK	CLKR
2	GA1	AIN–	10	TX. CLOCK	CLKX
3	GA2	GSX	11	RCV. SYNC	FSR
4	AGND	AGND	12	TX. SYNC	FSX
5	AOUT	AOUT	13	DGND	DGND
6	VREF	LOOP	14	PD	PND/BS
7	VDD	VDD	15	PCMOUT	DX
8	PCMIN	DR	16	VSS	VSS

Note:
DGSX: Transmit Gain Setting Data input pin
DGSR: Receive Gain Setting Data input pin

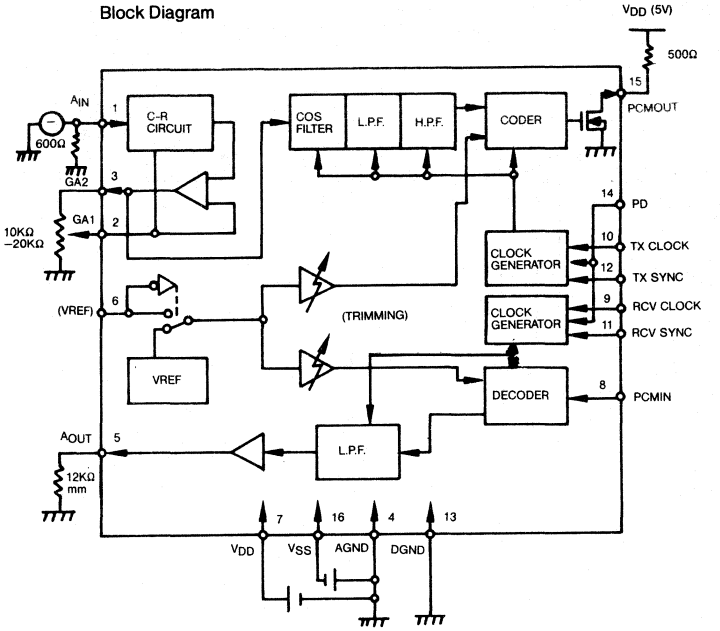
i) μPD9601D/μPD9602D

Block Diagram



ii) HD44233B/HD44234B

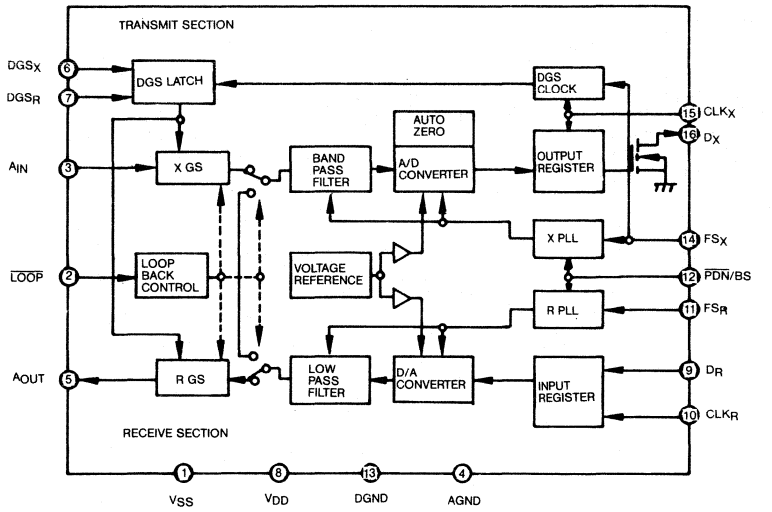
Block Diagram



Note: Pins no. 6, 11 and 12 are pulled up (NEC and Hitachi).

iii) μPD9604D/μPD9605D

Block Diagram



Note: pins no. 2, 6, 7, 11 and 14 are pulled up.

μPD960X Latch-up considerations

1. Power-up sequence

Our acceptable power-up sequence is as follows:

1. $V_{SS} - A_{GND} - D_{GND} - V_{DD}$ (same as Hitachi's way)
2. $V_{DD} - V_{SS} - A_{GND} + D_{GND}$ (same as μPD951x's way)
3. $V_{SS} - V_{DD} - A_{GND} + D_{GND}$ (ditto)
4. $A_{GND} + D_{GND} - V_{SS} - V_{DD}$ (ditto)
5. $V_{SS} - A_{GND} + D_{GND} - V_{DD}$ (ditto)

2. Latch-up for I/O pins

1. For input pins, over +/–20 mA can be applied as applied voltage is +/–50V.
2. For I/O and output pins, over +/–50mA can be applied.

3. Latch-up mechanism

Same as that of μPD951x.

Method to measure latch-up at CMOS COMBOS
This applies to μPD951X as well as to μPD960X.
- Method . . . . D.C. applied
- Limit 1, (For power supply pins)

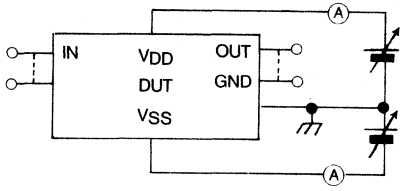
At T_a = 25°C, latch-up should not occur within absolute maximum ratings of power supply voltage.

(Cont'd)

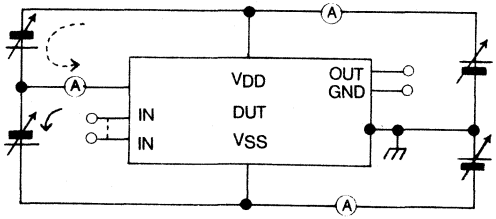
LIMIT 2, (FOR I/O PINS)
At T_a = 25°C, latch-up should not occur at input-current is ≦ 50 mA.
However, if latch-up will occur at less than 50 mA input-current, the following limits should be satisfied:
- For single power supply system.
  Latch-up should not occur at $-V_{DD}$ ≦ input voltage ≦ 2 x V_{DD}.
- For three power supplies system.
  $-2 \times V_{SS}$ ≦ input voltage ≦ 2 x V_{DD}

The evaluation circuits are as follows:

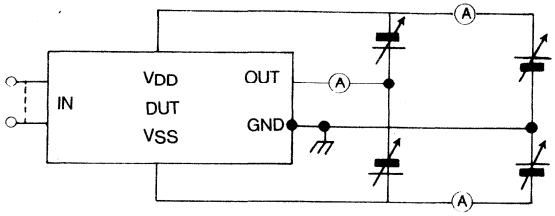
(A) For Power Pins



(B) For Input Pins



(C) For Output Pins



DUT: Device Under Test

RELIABILITY REPORT
μPD951xD / μPD960xD
PCM COMBO Families

μPD960XD Series

Test Item			Symbol	MIL-STD-883B. Method Cond.	Remarks	Observed Failures/ Test Samples			
						168h	500h	1000h	2000h
Life Test	High Temp. Operating		HTOL	1005 A,D	T_a = 150°C V_{DD} = 5.5V V_{SS} = −5.5V	0/137	0/137	0/137	0/20
Life Test	High Temp. Storage		HT	1008 D	T_a = 200°C	0/30	0/30	0/30	
Environmental Test	Thermal Stress	Soldering Heat	A 2	2031*	260°C, 10 sec, Once without flux	0/20			
Environmental Test	Thermal Stress	Temp. Cycling	A 2	1010 C	−65°C ~ 150°C (30 min) (30 min), 10 cycles	0/20			
Environmental Test	Thermal Stress	Thermal Shock	A 2	1011 A	0°C ~ 100°C (5 min) (5 min), 15 cycles	0/20			
Environmental Test	Thermal Stress	Hermeticity	A 2	1014 B,C	1 x 10^{-8} atm : cc/sec	0/20			
Environmental Test	Mechanical Stress	Mechanical Shock	A 3	2002 B	1500G, 0.5msec, 3times 3 directions	0/20			
Environmental Test	Mechanical Stress	Vibration var. frg.	A 3	2007 A	100~2000~100Hz, 20G, 4times 3 directions	0/20			
Environmental Test	Mechanical Stress	Constant Accelaration	A 3	2001 D	20,000G, 1min, Once 3 directions	0/20			
Environmental Test	Mechanical Stress	Hermeticity	A 3	1014 B,C	1 x 10^{-8} atm : cc/sec	0/20			
Environmental Test	Terminal Strength (Lead Fatigue)		A 4	2004 B2	250 g, 3 leads, 3bends	0/5			
Environmental Test	Solderability		A 5	2003	230°C, 5 sec, Once with flux	0/5			

*MIL-STD-750A

μPD951XD Series

Test Item			Symbol	MIL-STD-883B. Method Cond.	Remarks	Observed Failures/ Test Samples			
						168h	500h	1000h	2000h
Life Test	High Temp. Operating		HTOL	1005 A,D	T_a = 150°C V_{DD} = 5.5V V_{SS} = −5.5V	0/110	0/90	0/48	0/20
Life Test	High Temp. Storage		HT	1008 D	T_a = 200°C	0/20	0/20	0/20	
Environmental Test	Thermal Stress	Soldering Heat	A 2	2031*	260°C, 10 sec, Once without flux	0/20			
		Temp. Cycling		1010 C	−65°C ~ 150°C (30 min) (30 min) 10 cycles				
		Thermal Shock		1011 A	0°C ~ 100°C (5 min) (5 min) , 15 cycles				
		Hermeticity		1014 B,C	1 x 10^{-8} atm : cc/sec				
	Mechanical Stress	Mechanical Shock	A 3	2002 B	1500G, 0.5msec, 3times 3 directions	0/20			
		Vibration var. frg.		2007 A	100~2000~100Hz, 20G, 4times 3 directions				
		Constant Accelaration		2001 D	20,000G, 1min, Once 3 directions				
		Hermeticity		1014 B C	1 x 10^{-8} atm : cc/sec				
	Terminal Strength (Lead Fatigue)		A 4	2004 B 2	250 g, 3 leads, 3bends	0/5			
	Solderability		A 5	2003	230°C, 5 sec, Once with flux	0/5			

*MIL-STD-750A

μPD6302CA
μPD6302G
MSK MODEM

METHOD OF USING μPD6302CA/G MSK MODEM

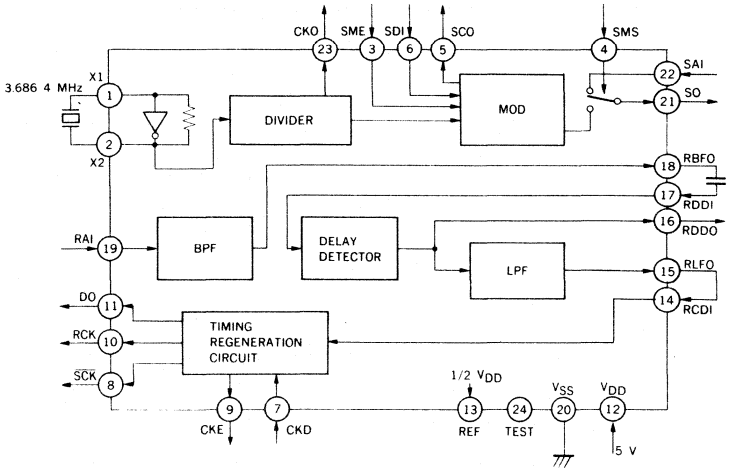
1. Outline of μPD6302CA

The μPD6302CA/G is a one-chip CMOS IC used to modulate/demodulate the Minimum Shift Keying (MSK) signal to/from Non Return Zero (NRZ) code (high level – 1.2 kHz, low level – 1.8 kHz).

The modulator section has a transmitted clock output terminal and a transmitted data input terminal, and the built-in modulation select switch switches between the audio signal and modulation signal.

The demodulator section has a band pass filter and a low pass filter composed of switched-capacitor filters (SCFs) as detection filters, regenerated clock terminal to output the signal from the bit synchronization circuit, and reproduced data output terminal.

BLOCK DIAGRAM



TERMINAL

1 ... X1	OSC IN	13 ... REF	REFERENCE OUT
2 ... X2	OSC OUT	14 ... RCDI	CLOCK DEMODULATER IN (RECEIVING)
3 ... SME	MODULATION ENABLE (SENDING)	15 ... RLFO	LOWPASS FILTER OUT (RECEIVING)
4 ... SMS	MODULATION SELECT (SENDING)	16 ... RDDO	DELAY DETECTOR OUT (RECEIVING)
5 ... SCO	CLOCK OUT (SENDING)	17 ... RDDI	DELAY DETECTOR IN (RECEIVING)
6 ... SDI	DATA IN (SENDING)	18 ... RBFO	BAND PASS FILTER OUT (RECEIVING)
7 ... $\overline{CKD}$	SERIAL CLOCK DISENABLE IN	19 ... RAI	RECEIVED AUDIO IN
8 ... $\overline{SCK}$	SERIAL CLOCK OUT	20 ... V_{SS}	GND
9 ... CKE	SERIAL CLOCK ENABLE OUT	21 ... SO	SENDING OUT
10 ... RCK	CLOCK OUT (RECEIVING)	22 ... SAI	SENT AUDIO IN
11 ... DO	DATA OUT (RECEIVING)	23 ... CKO	CLOCK OUT
12 ... V_{DD}	+5V	24 ... TEST	TEST

2. MINIMUM SHIFT KEYING (MSK)

The MSK is one of the frequency modulation (FM). With this method, the high level (logic level) and low level of the NRZ code are modulated to 1.2kHz and 1.8kHz respectively.

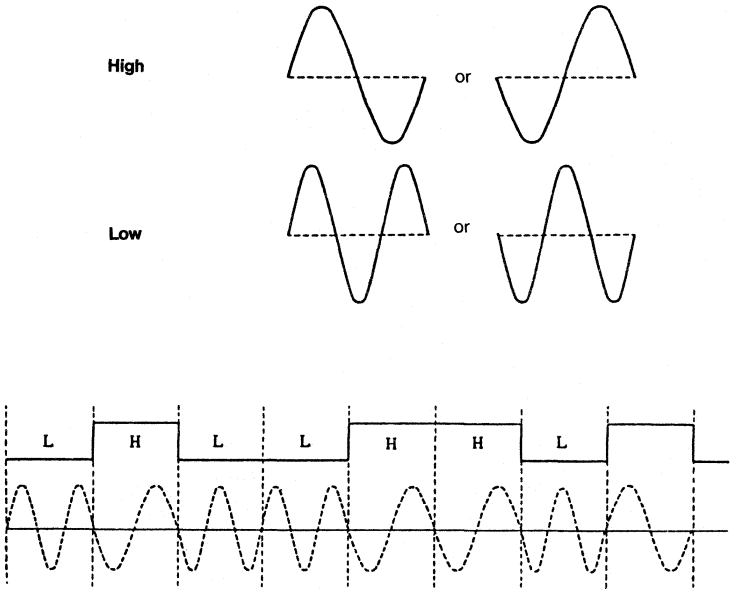


Fig. 1 Example of modulation by MSK method

3. FUNCTIONS OF μPD6302CA

3.1 Modulator section

The NRZ data code generated by the micro computer is read into μPD6302CA/G from the SDI terminal according to the rising edge of the clock (SCO) from the μPD6302CA/G when the SME terminal is set to high level. Then, the high level of the NRZ code is modulated to a 1.2 kHz sine wave, and the low level is modulated to a 1.8 kHz sine wave. The modulated signal is output from the SO terminal. Normally, an audio signal from the SAI terminal is output from the SO terminal. Therefore, when data is to be transmitted, the output from the SO terminal must be switched from the audio signal to the modulated signal by the input of a control signal to the SMS terminal.

3.2 Demodulator section

When a received signal is input from the RAI terminal, the out-of-band noise is removed from it by the band pass filter. Then, the signal is output from RBFO terminal and input to the RDDI terminal.

The signal input to the RDDI terminal passes through the 48-bit shift delay detection circuit and the low pass filter to remove the pulse wave generated by delay detection; then, it is output from the RLFO terminal.

This signal is then input from the RCDI terminal, into the logic level by the comparator, synchronized with the internal clock by the clock regenerate circuit, and output from the DO terminal.

3.3 Frame synchronization detector section

The frame synchronization signal detection circuit, which is a part of the demodulation circuit, detects a 15-bit frame (frame pattern: 1 1 1 0 1 1 0 0 1 0 1 0 0 0 0 : disprogrammable) synchronization signal (all match) from the demodulated NRZ signal, raises the signal from CKE to a high level to indicate the detection, and outputs a 1.2 KHz serial clock signal from the $\overline{SCK}$ terminal. The signals output from CKE and $\overline{SCK}$ are reset when the signal input to the CKD terminal is set to a high level.

With this circuit, the frame synchronization signal need not be detected by the software. (See Figure 11 and Flowchart 3 for details).

4. RECEIVE DEMODULATOR SECTION

4.1 Band pass filter (BPF)

The band width is from 800 Hz to 2.2 KHz (typ.). The attenuation slope is 24 dB/oct (typ.), and the in band attenuation is 10 dB (typ.). The band pass filter removes the out-of-band noise.
(Fig.2)

4.2 Low pass filter (LPF)

The cut off frequency is 700 Hz (typ.), and the attenuation slope is 18 dB (oct (typ.), and the inband attenuation is 7 dB (typ.).

The low pass filter removes the pulse wave generated by a shift detection.
(Fig. 3)

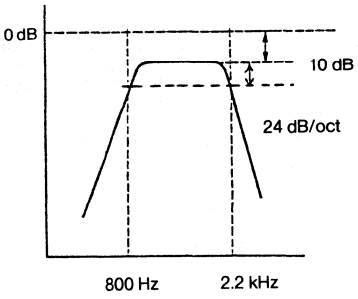


Fig. 2 BPF

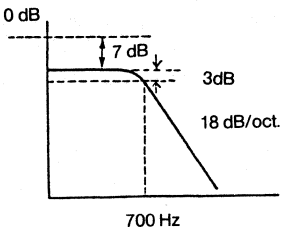


Fig. 3 LPF

4.3 Bit synchronization circuit

The bit synchronization circuit regenerates clock synchronized with the received data. At least 24 received data transitional points are necessary to regenerate received clock. (The lock-in range is from 1.160 baud to 1.250 baud TYP).

4.4 Frame code detection

The frame code detection detects the 15-bit frame code (1 1 1 0 1 1 0 0 1 0 1 0 0 0 : fixed code).

This circuit outputs a high level signal from CKE as the detection signal and a serial clock signal from $\overline{SCK}$. The detection condition is the matching of all 15 bits.
(Fig. 4)

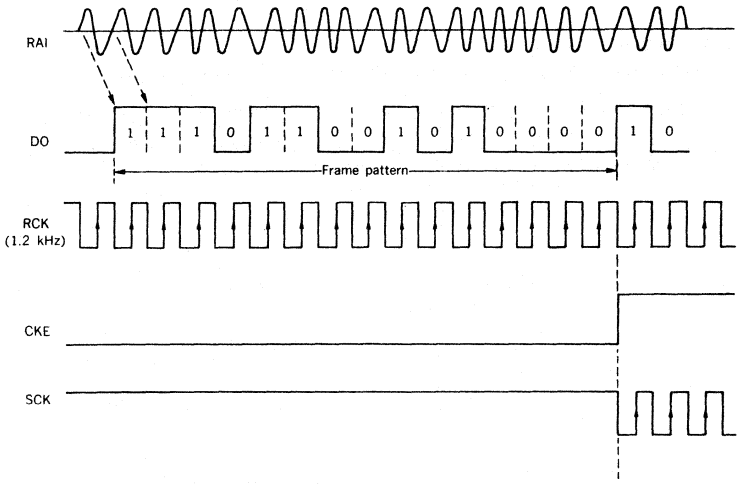


Fig. 4 Frame detector

* Note: it is possible to modify the frame pattern of synchro detection circuit by optional aluminium mask. In this case development costs and a minimum quantity are necessary.

5. Modulator Section

5.1 Data input

The data from the microcomputer is input to SDI and is latched in μPD6302CA/G by the rising edge of the transmitted clock (SCO) output).

If the microcomputer holds the data for at least 10 μs before and after the rising of the transmitted clock, the data is read into the IC. (Fig. 6)

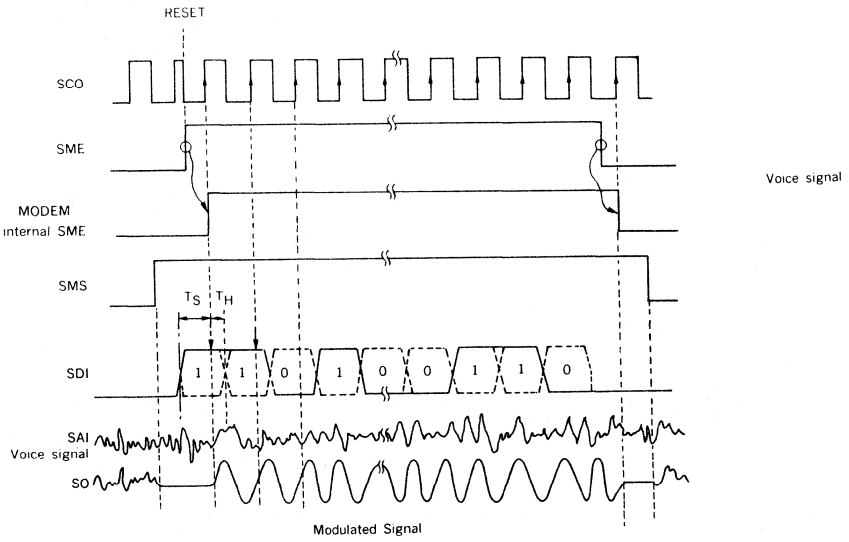
Data setup Time: 10 μs (min.)
Data hold time: 10 μs (min.)

5.2 Modulated data output

Modulation is started when the signal input to the SME terminal is set to a high level.

This signal is latched in the IC by the rising edge of the SCO signal, and the data transmission mode is started.

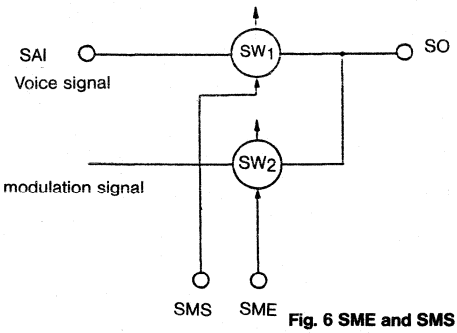
Note: The transmitted clock (SCO output) is reset for about 2 μs typ unconditionally after the SME signal rises.
Fig. 5 shows the timing chart, and Fig. 6 shows the truth table for SME and SMS.
For reference, Fig. 7 shows the input/output terminal interface.



T_S : Set-up time MIN. 10 μs

T_H : Hold time MIN. 10 μs

Fig. 5 SME, SMS Timing Diagram



SME	SMS	SW_1	SW_2	SO output
L	L	ON	OFF	SAI
L	H	OFF	OFF	1/2 V_{DD}
H	L	OFF	ON	D/A
H	H	OFF	ON	D/A

Note: SME and SMS can be controlled in the same port.

Fig. 6 SME and SMS truth table

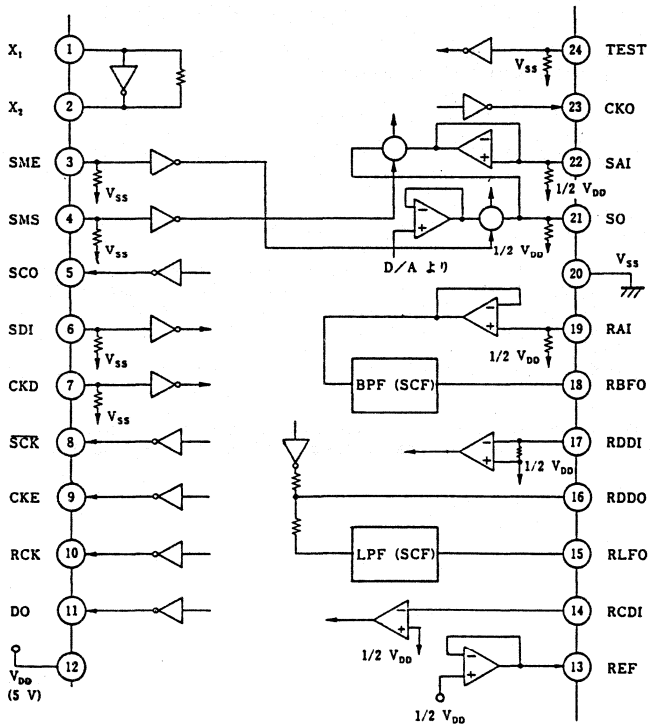


Fig. 7 Terminal interface

output inpedance

RBFO ..... 3.5 (kΩ)
RLFO ..... 5.0 (kΩ)
REF ..... 4.0 (kΩ)
SO (D/A) ..... 700 (Ω)
SO (SAI) ..... 300 (Ω)

6. PROGRAM (MICROCOMPUTER)

6.1 Transmit program

The send data is latched in μPD6302CA/G by the rising of the transmitted clock (SCO output) and is modulated. For this purpose, the program must instruct the microcomputer to hold the data for 10μs before and after the rising edge of the SCO clock.

Note that SCO output control terminal SMS and transmit control terminal SME can be controlled by one port.

6.2 Receive program

The received data is transformed by the falling edge of the RCK (regeneration clock), since the transformed data is held for 1 clock cycle read it by the interruption at the rising edge of the RCK clock. (See Flowchart 1, Fig. 8).

When frame pattern detection circuit is used, a high level signal is output from the CKE terminal and a serial clock signal is output from the $\overline{SCK}$ terminal to indicate detection of a frame pattern.

These signals are output immediately after a frame pattern is detected.

Thus, frame pattern detection need not be performed by software. That is, the micro computer reads the data the rising edge of the serial clock when the detection signal (used as interruption signal) is output from the CKE terminal. (See flowchart 2, Fig. 9)

This processing can be further simplified by using a serial interface in a device such as μPD7508.

With this serial interface (Fig. 10), interruptions (CKE output) need not be monitored by software because the interruption signal is generated from a 3-bit counter by hardware. That is, immediately after a frame pattern is detected, data is latched in an 8-bit shift register by the serial clock output from the $\overline{SCK}$ terminal, and the 3-bit counter starts counting. When 8-bit data is set in the 8-bit shift register, the 3-bit counter issues an interruption signal.

On receiving this signal, the CPU of the microcomputer reads the 8-bit data from the 8-bit shift register via the internal bus (See Flowchart 3).

Since the microcomputer reads the demodulated data by the repetition of this operation, no special processing (frame pattern detection) for data code detection is required and the received data is read not at every $\overline{SCK}$ (SCO) clock but at every 8 $\overline{SCK}$ clocks.

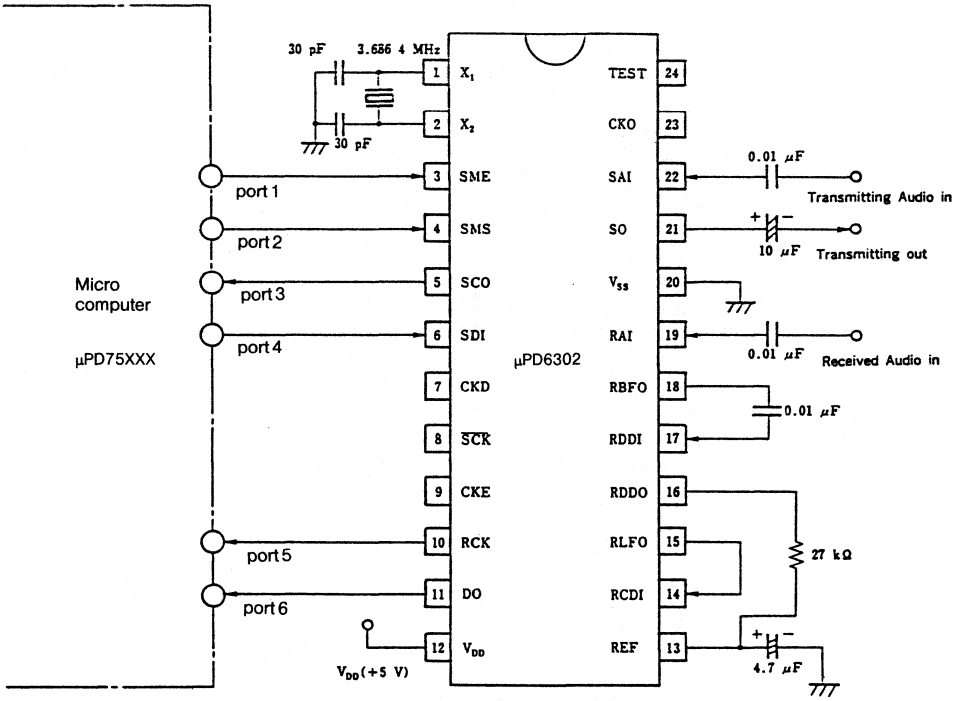
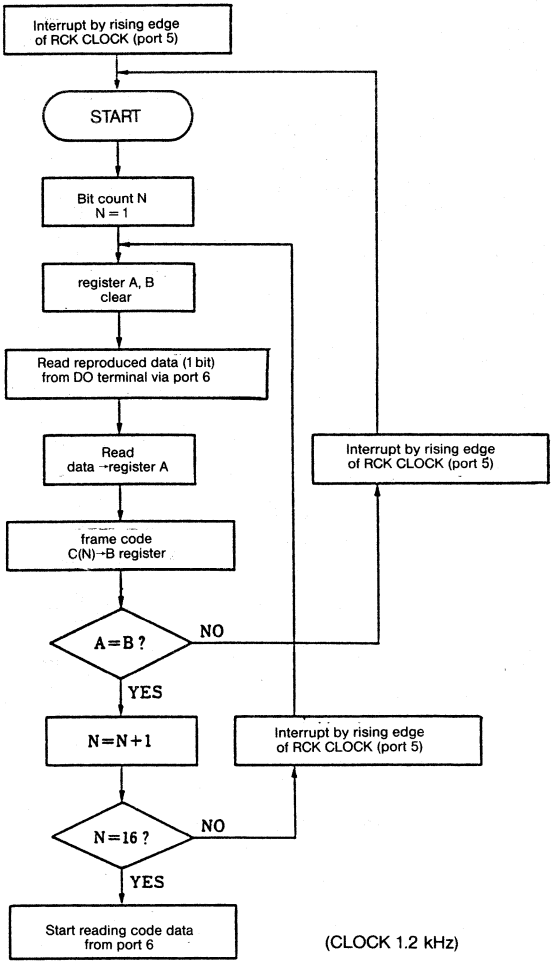


Fig. 8 Interface with microcomputer



Flowchart 1

Note: C (1) to C (15) are used to contain the 15-bit frame synchronization signal, 1 bit each, starting from the first bit.

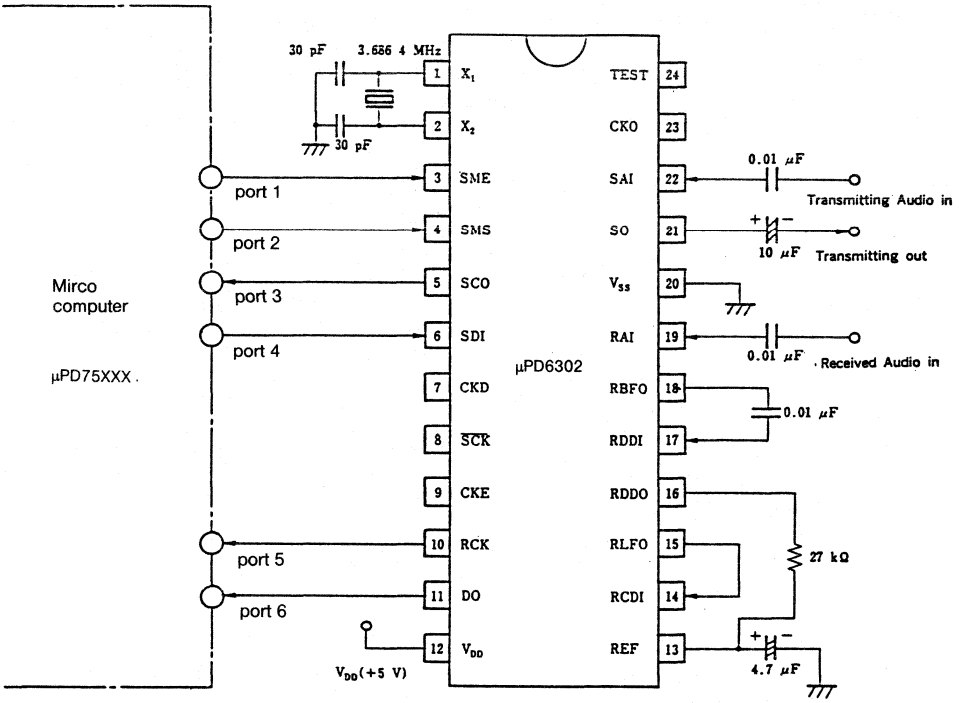
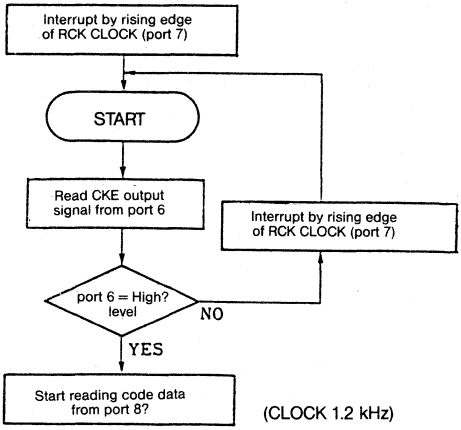


Fig. 9 Interface with microcomputer



Flowchart 2

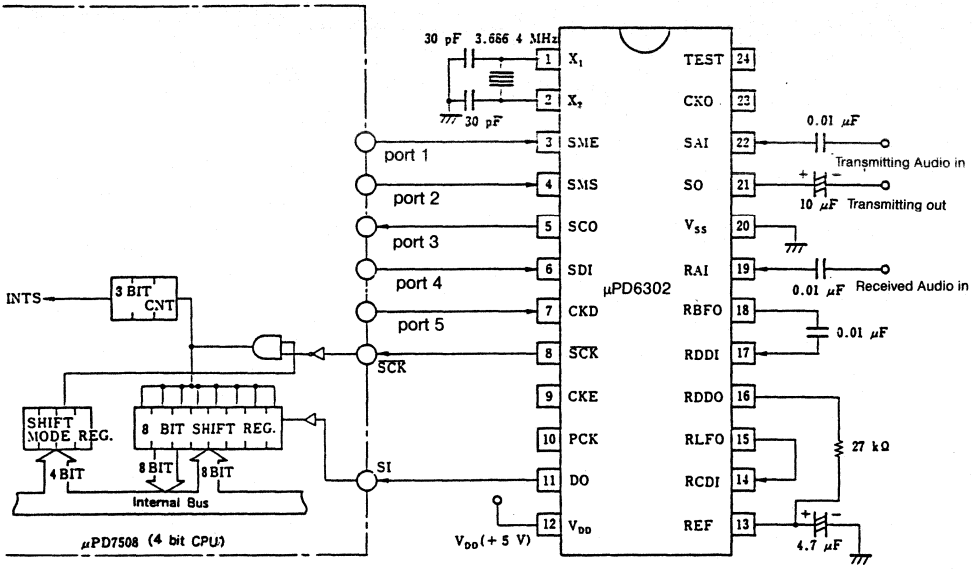
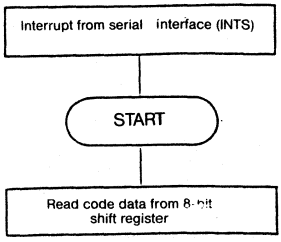


Fig. 10 Interface with microcomputer

In this case, an interruption is generated by the hardware when a frame code is detected, and no special program is necessary for detecting the frame code.



Flowchart 3

MSK MODEM μPD6302CA/G FUNCTION

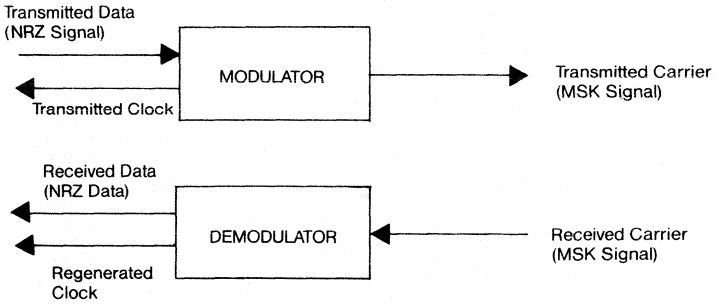


Figure 1

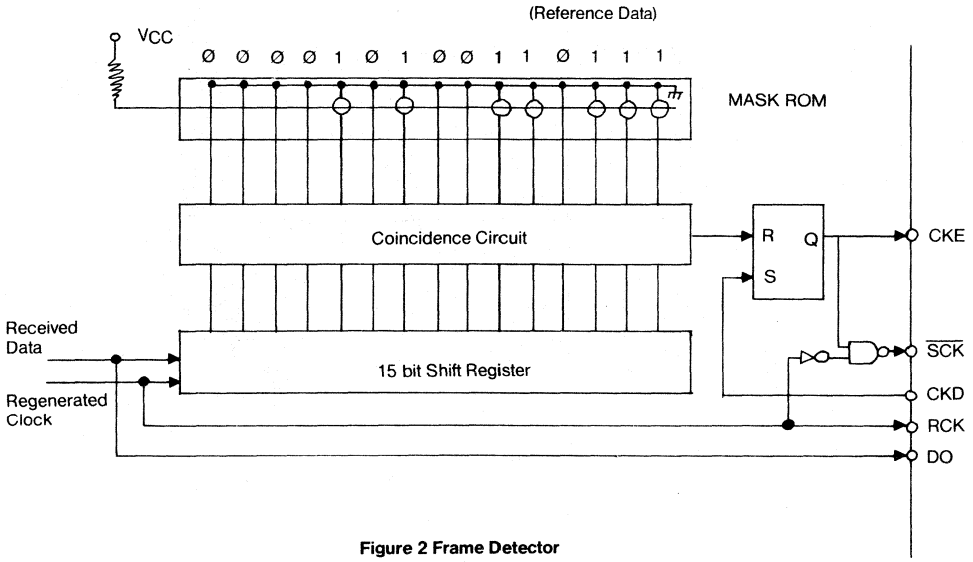
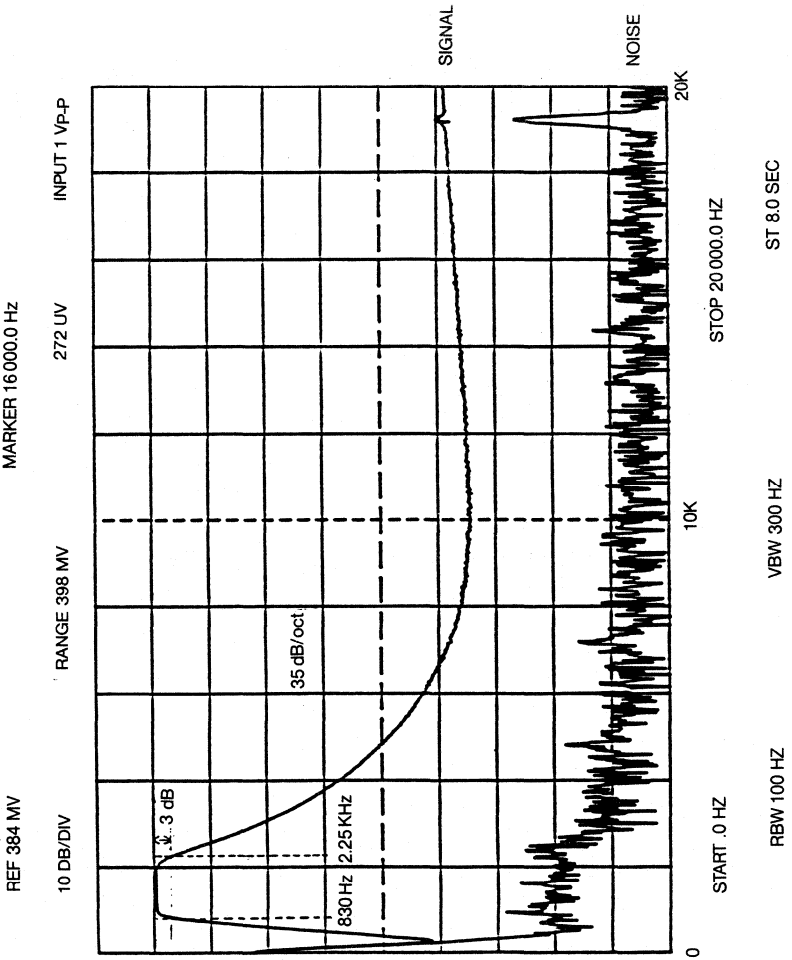


Figure 2 Frame Detector

Fig. 3 BPF CHARACTERISTIC μPD6302CA



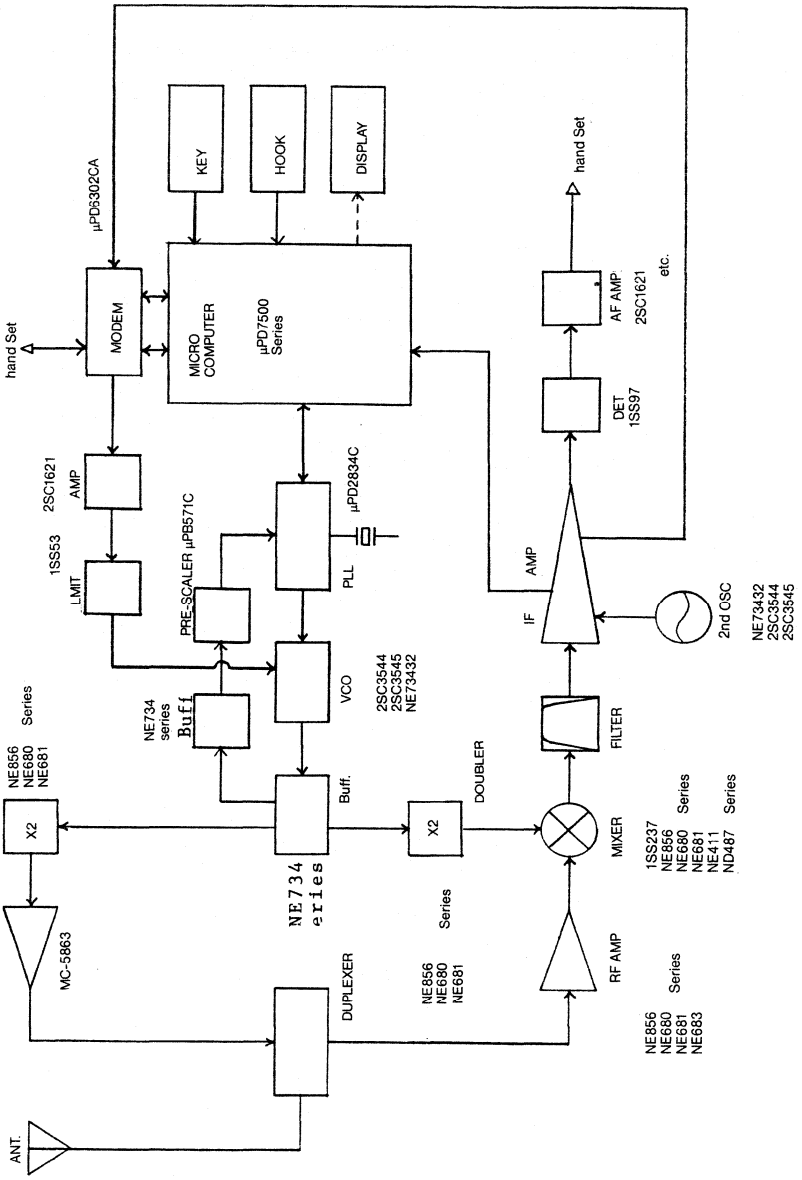


Fig. 4 CORD LESS TELEPHONE BLOCK DIAGRAMM
For EUROPE (CEPT) (914/959MHz)

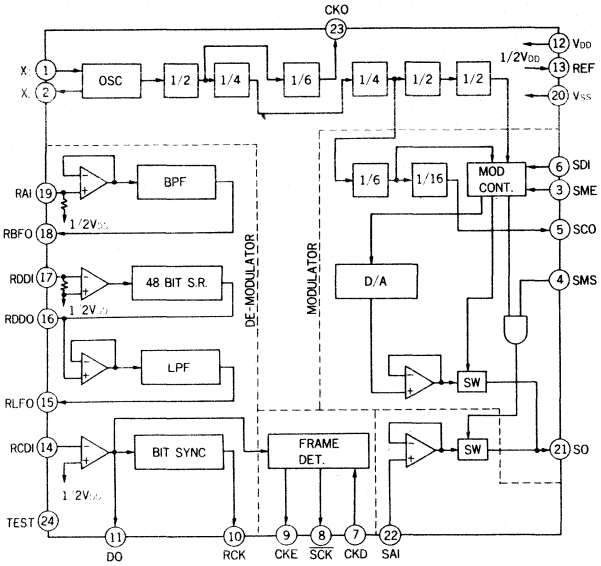


Fig. 5 Block diagram of μPD6302CA. (details)

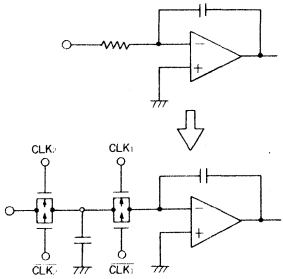


Fig. 6 Switched capacitor integrator.

Performance of the SCF (Switched Capacitor Filters)
Two SCF, one LPF and one BPF, are integrated with following parameters:

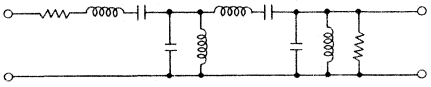


Fig. 7 LCR circuit equivalent to the SCF (BPF).

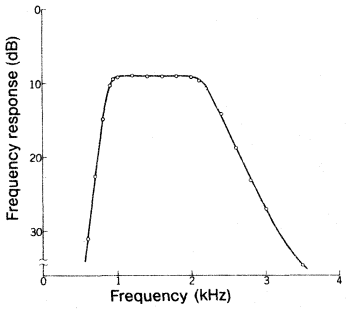


Fig. 8 Frequency characteristics of BPF.

BPF: 4th order Tschebycheff, 9dB loss, bandwidth 850Hz to 2,5 kHz and 36,5 dB/oct roll-off.
Its role is to pass the 1,2 kHz and 1,8 kHz signal and eliminate the out-of-band noise.

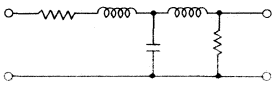


Fig. 9 LCR circuit equivalent to the SCF (LPF).

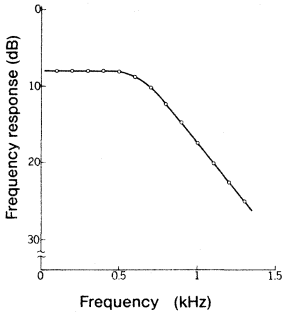


Fig. 10 Frequency characteristics of LPF.

LPF: 3rd order Tschebycheff, 8 dB loss,bandwidth DC to 750 Hz and 17,4 dB/oct roll-off.

Its role is to eliminate, spurious wich is created in the signal after the 48 bit Delay Detector Block of the μPD6302

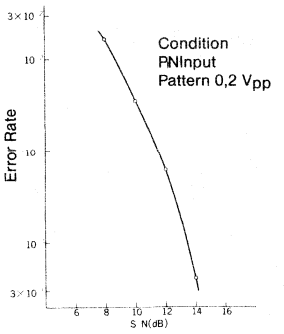


Fig. 11 Error rate characteristics of μPD6302CA.

DESCRIPTION

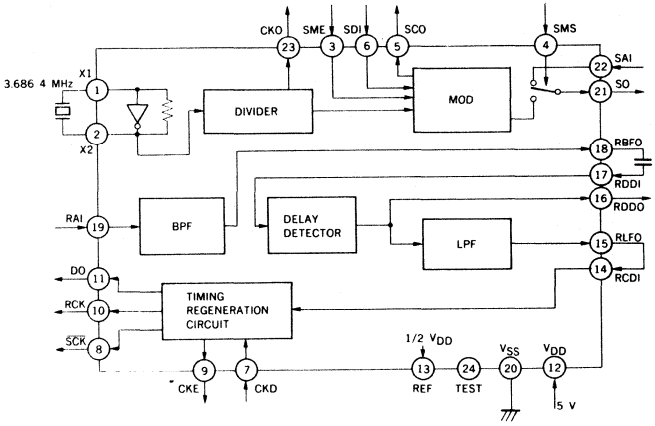
μPD6302CA, μPD6302G a single-chip CMOS LSI, consists of a modulator and a demodulator with a frame code detection circuit included.

It is ideal as MODEM for MSK (Minimum Shift Keying) system personal radio, MCA and codeless telephone.

FEATURES

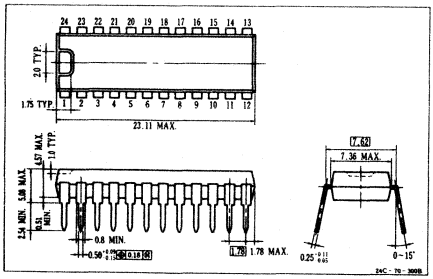
- Incorporates SCF receiving filter circuit
- Incorporates frame code detecter, which reduces the software load of the controller
- Regenerated data can be transferred by serial interface of microconputer
- Incorporates 307 kHz clock output for CPU
- Incorporates switching circuit to exchange voice signal for modulated data signal
- 5 V single power supply
- Low power consumption achieved by CMOS process
- Compact 24-pin shrink DIP (Dual Inline Package) or 24-pin miniflat Package

BLOCK DIAGRAM

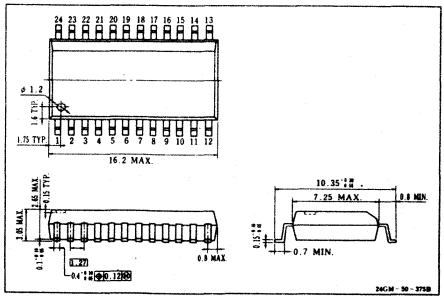


PACKAGE DIMENSIONS (Unit: mm)

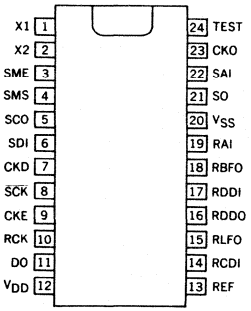
μPD6302CA
24 PIN SHRINK DIP (300 mil)



μPD6302G
24 PIN MINIFLAT



CONNECTION DIAGRAM (Top view)



1 ... X1 OSC IN
2 ... X2 OSC OUT
3 ... SME MODULATION ENABLE (SENDING)
4 .. SMS MODULATION SELECT (SENDING)
5 ... SCO CLOCK OUT (SENDING)
6 ... SDI DATA IN (SENDING)
7 ... CKD SERIAL CLOCK DISENABLE IN
8 ... $\overline{SCK}$ SERIAL CLOCK OUT
9 ... CKE SERIAL CLOCK ENABLE OUT
10 ... RCK CLOCK OUT (RECEIVING)
11 ... DO DATA OUT (RECEIVING)
12 ... V_{DD} +5 V
13 ... REF REFERENCE OUT
14 ... RCDI CLOCK DEMODULATER IN (RECEIVING)
15 ... RLFO LOWPASS FILTER OUT (RECEIVING)
16 ... RDDO DELAY DETECTOR OUT (RECEIVING)
17 ... RDDI DELAY DETECTOR IN (RECEIVING)
18 ... RBFO BAND PASS FILTER OUT (RECEIVING)
19 ... RAI RECEIVED AUDIO IN
20 ... V_{SS} GND
21 ... SO SENDING OUT
22 ... SAI SENT AUDIO IN
23 ... CKO CLOCK OUT
24 ... TEST TEST

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Supply voltage	$V_{DD} - V_{SS}$	7.0	V
Input voltage	$V_{IN} - V_{SS}$	−0.3 to V_{DD} +0.3	V
Power consumption	P_D	350	mW
Operating temperature	T_{OPT}	−40 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITION (T_a = 25°)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Oscillation frequency	f_{osc}		3.686 4		MHz
Received signal input level	V_{IN} (RAI)	0.2	0.3	1.0	V_{p-p}
Voice signal input level	V_{IN} (SAI)		1	1.5	V_{p-p}

ELECTRICAL CHARACTERISTICS (T_a = 25°C, V_{DD} = 5V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Current consumption	I_{DD}	2.5	4.2	5.5	mA	
High level input voltage	V_{IH}	0		0.3 V_{DD}	V	(SME, SDI, TEST, CKD, SMS)
Low level input voltage	V_{IL}	0.7 V_{DD}		V_{DD}	V	(SME, SDI, TEST, CKD, SMS)
Input pull-down resistance	R_{IN}	100	200	350	kΩ	(SME, SDI, TEST, CKD, SMS)
Input leak current	I_{IH}			+2	μA	V_{IN} = 5 V (RCDI)
Input leak current	I_{IL}			−2	μA	V_{IN} = 0 V (RCDI)
Input impedance	R_{IN}	100	200	350	kΩ	(RDDI, SAI, RAI)
High level output voltage	V_{OH}	V_{DD} − 1		V_{DD}	V	I_{OH} = 0.5 mA
Low level output voltage	V_{OL}	0		1	V	I_{OL} = −0.5 mA (RCK, DO, CKE, $\overline{SCK}$, RDDO, CKO)
Sending output impedance	R_{SO}			5	kΩ	
Voice input amplifier gain	A_{AF}	−1.0	−0.3	+0.5	dB	
Sending output amplitude	V_{SO}	0.8	1.0	1.2	V_{p-p}	
Oscillation feedback resistance	R_{fx}	500	1 000	2 000	kΩ	

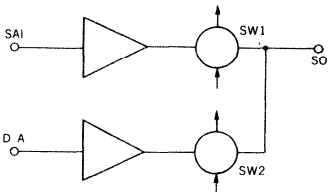
EXPLANATION OF INPUT AND OUTPUT TERMINALS

X1, X2	These terminals are for connection to a 3.686 4 MHz crystal.
SME (Note 1)	Controls whether or not the modulated data signal will be output to the sending output terminal (SO). The modulated data signal is output at "H" level, and 1/2 V_{DD} DC Voltage is output at "L" level, in synch with the SCO clock (when the SMS terminal is "H").
SMS (Note 1)	Controls whether the voice signal or modulated data signal is output to the sending output terminal (SO). The voice signal from SAI is output at "L" level, and the internal modulated signal is output at "H" level.
SCO	Clock output for transmitting demodulated data signal is applied from SDI in synch with this clock. (Frequency: 1.2 kHz)
SDI	Sending data inputs in synch with the SCO clock.
CKD	Serial interface control terminal stops serial clock output ($\overline{SCK}$) when CKD is "H", and puts back the CKE terminal to "L" level.
$\overline{SCK}$	Clock for serial interface output. This received clock output is controlled by the frame detection circuit; the clock output is started upon detection of frame pattern match, and stopped by an external CKD input signal.
CKE (Note 2)	Serial interface control output. This output is set to "H" level when frame pattern match is detected by the frame detection circuit. This output is reset by CKD input.
RCK	Outputs the regenerated clock (1.2 kHz) in synch with the received data signal.
DO	Outputs the received data signal in synch with the regenerated clock (RCK).
V_{DD}	+5 V supply
REF	Outputs 1/2 V_{DD}, the mid-point voltage of power supply.
RCDI	Bit synchronous circuit input. Normally, it directly inputs the RLFO output.
RLFO	Outputs low-pass SCF after delay detection.
RDDO	Control terminal of delay detector output level. Normally, it connects with REF terminal through a resistor (27 KΩ).
RDDI	Delay detector input. Normally, RBFO output is applied this terminal through 0.47 μF capacitor.
RBFO	Output of Band pass filter.
RAI	Band pass filter input. It inputs received signal.
V_{SS}	Ground (0 V)
SO	Sending signal output. It outputs the internal modulation signal (staircase/sine wave output, 1.2 or 1.8 kHz) or the voice signal input from SAI terminal.
SAI	Voice signal input terminal for outputting voice signal to the send output terminal (SO).
CKO	Outputs clock to the external CPU. (Frequency: 307.2 kHz)
TEST	When this terminal is "H", each IC function can be tested. Normally, this terminal is open or connected to V_{SS} (Ground).

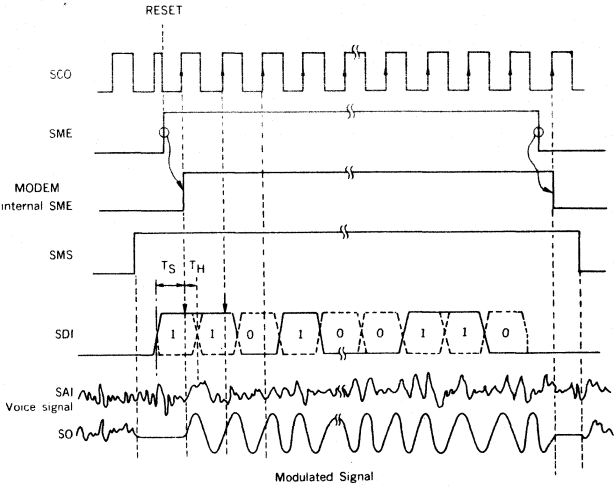
(Note 1)

SME and SMS truth table

SME	SMS	SW1	SW2
L	L	ON	OFF
L	H	OFF	OFF
H	L	OFF	ON
H	H	OFF	ON



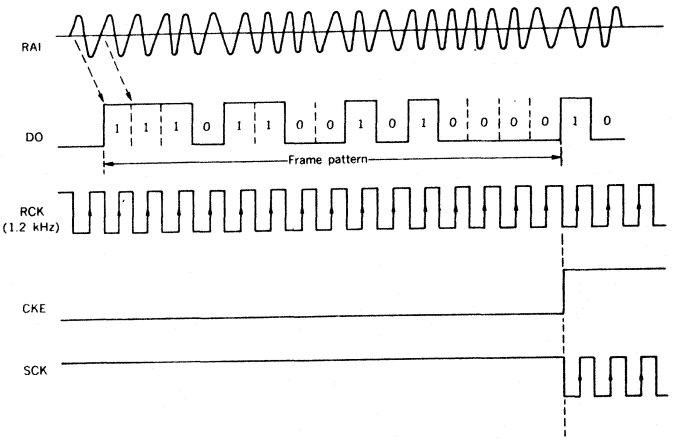
SME, SMS Timing Diagram (Note 1)



T_S : Set-up time MIN. 10 μs

T_H : Hold time MIN. 10 μs

CKE Timing Diagram (Note 2)



FUNCTION EXPLANATION

μPD6302CA, μPD6302G can be functionally divided into modulator, demodulator, and frame detector.

DEMODULATOR

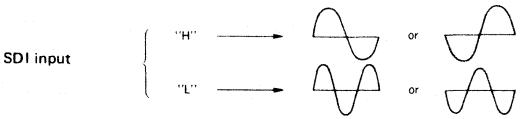
The MSK modulated wave input to RAI is passed through the internal BPF, where out-band noise is removed, and it is output to RBFO.

The signal from RBFO is input into RDDI and then passed through the 48-bit shift detector and LPF to be transformed to the logic level.

The transformed signal is output as the demodulated NRZ signal and regenerated clock by the bit synchronous circuit in synch with the internal clock.

MODULATOR

The NRZ signal input from SDI is transformed to 1.2 kHz sine wave at "H" level, and 1.8 kHz sine wave at "L" level by the modulator.



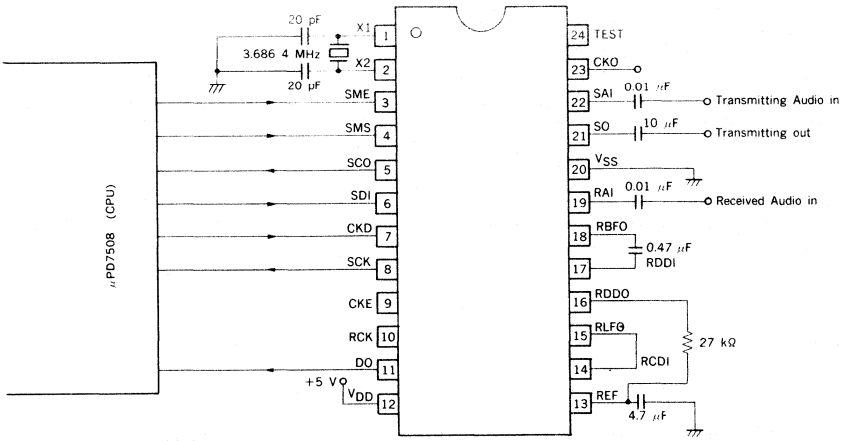
The modulated signal is output from SO, which is controlled by the SME and SMS terminal inputs. (Note 1)

FRAME DETECTOR

Frame pattern is detected from the NRZ signal demodulated by the demodulator. When the frame pattern is detected, the CKE terminal outputs "H" level signal, and the $\overline{SCK}$ terminal outputs 1.2 kHz serial clock signal, until an "H" level signal is input into the CKD terminal. (Note 2)

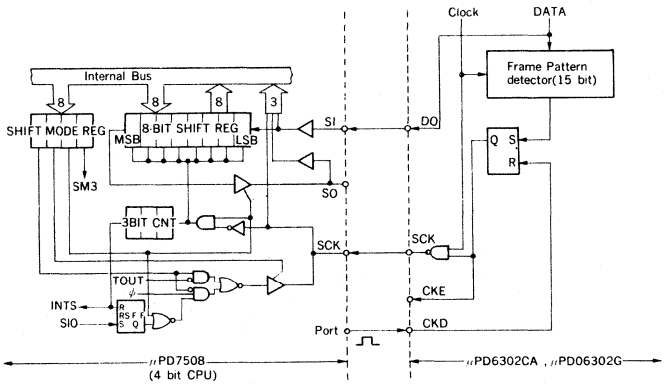
APPLICATION CIRCUIT

1. Interface with μPD7508



Note : SME and SMS can be controlled in the same port.

2. Serial interface of received data (frame detector circuit)



μPD7720A
μPD77C20A
μPD77P20

DIGITAL SIGNAL PROCESSOR

Mask-ROM

μPD7720AC (NMOS plastic)
μPD7720AD (NMOS ceramic)
μPD7720AL (NMOS PLCC)

μPD77C20AC (CMOS plastic)
μPD77C20AD (CMOS ceramic)
μPD77C20AL (CMOS PLCC)

UV-EPROM

μPD77P20D (NMOS cerdip)

Description

The μPD7720A and μPD77P20, two signal processing interface (SPI) chips that are functionally the same, are advanced architecture microcomputers optimized for signal processing algorithms. Their speed and flexibility allow these SPIs to efficiently implement signal processing functions in a wide range of environments and applications.

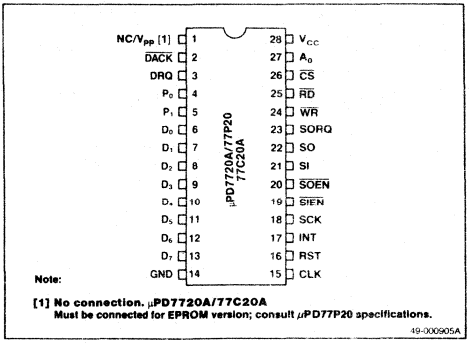
The μPD7720A, a revision of the μPD7720, the original mask ROM chip, uses a third less power than the μPD7720. The μPD77P20 is an ultraviolet erasable and electrically programmable (EPROM) version of the μPD7720A. Program and data ROM, masked for the μPD7720A, are implemented in EPROM for the μPD77P20. The μPD77P20 is useful in prototype applications or in systems where product quantities are insufficient for masked ROM development. Since the inception of μPD7720 and its companion EPROM version, μPD77P20, there have been several mask revisions to improve either/both manufacturability and/or function. A μPD77P20 must always be used to verify function of a user's system before submitting ROM code for μPD7720A, but certain early versions of μPD77P20 must not be used for final verification. Please refer to the section on μPD77P20 for details.

Features

- ☐ Fast instruction execution—250 ns
- ☐ 16-bit data word
- ☐ Multi-operation instructions for optimizing program execution
- ☐ Large memory capabilities:
  - — Program ROM (512 x 23 bits)
  - — Data ROM (510 x 13 bits)
  - — Data RAM (128 x 16 bits)
- ☐ Fast (250 ns) 16-bit multiplier (31 bits)
- ☐ Dual accumulators
- ☐ Four-level subroutine stack for program efficiency
- ☐ Multiple I/O capabilities:
  - — Serial
  - — Parallel
  - — DMA
- ☐ Compatible with most microprocessors, including:
  - — μPD8080
  - — μPD8085
  - — μPD8086
  - — μPD780 (Z80®)
- ☐ Power supply +5 V
- ☐ NMOS technology
- ☐ Extended temperature versions available.

® Z80 is a registered trademark of Zilog Corporation.

Pin Configuration



Note:

[1] No connection. μPD7720A/77C20A
Must be connected for EPROM version; consult μPD77P20 specifications.

49-000905A

Applications

- ☐ Digital filtering
- ☐ High-speed data modems
- ☐ Fast Fourier transforms (FFT)
- ☐ Speech synthesis and analysis
- ☐ Dual-tone multi-frequency (DTMF)
- ☐ Equalizers
- ☐ Adaptive control
- ☐ Numerical processing

Performance Benchmarks

- ☐ Second order digital filter (biquad): 2.25 μs
- ☐ μ/A law to linear conversion: 0.50 μs
- ☐ FFT, 32-point complex: 0.7 ms
  64-point complex: 1.6 ms

Ordering Information

Part Number	Package Type	Max Frequency of Operation	Normal Temperature Range
μPD7720AD	28-Pin ceramic DIP	8.33 MHz	−10°C to 70°C
μPD7720AC	28-Pin plastic DIO	8.33 MHz	−10°C to 70°C
μPD7720AL	44-Pin PLCC	8,33 MHz	−10°C to 70°C
μPD77C20AD	28-Pin ceramic	8,33 MHz	−40°C to 85°C
μPD77C20AC	28-Pin plastic	8,33 MHz	−40°C to 85°C
μPD77C20AL	44-Pin PLCC	8,33 MHz	−40°C to 85°C
μPD77P20D	28-Pin cerdip	8.196 MHz	−10°C to 70°C

Pin Identification

No.	Symbol	Function
1	NC/V_{PP}	No connection (μPD7720A, 77C20A)/ Programming voltage (μPD77P20)
2	$\overline{DACK}$	DMA request acknowledge input
3	DRQ	DMA request output
4, 5	P_0, P_1	General purpose output control lines
6-13	D_0-D_7	Three-state I/O data bus
14	GND	Ground
15	CLK	Single phase master clock input
16	RST	Reset input
17	INT	Interrupt input
18	SCK	Serial data I/O clock input
19	$\overline{SIEN}$	Serial input enable input
20	$\overline{SOEN}$	Serial output enable input
21	SI	Serial data input
22	SO	Three-state serial data output
23	SORQ	Serial data output request
24	$\overline{WR}$	Write control signal input
25	$\overline{RD}$	Read control signal input
26	$\overline{CS}$	Chip select input
27	A_0	Status/data register select input
28	V_{CC}	+5 V power supply

Pin Functions

NC/V_{PP}

This pin is not internally connected in the μPD7720. In the μPD77P20, this pin inputs the programming voltage (V_{PP}) when the part is being programmed.

This pin must be connected for proper μPD77P20 operation. Consult the section on the μPD77P20 for details.

$\overline{DACK}$ [DMA Request Acknowledge]

This input indicates to the μPD7720 that the data bus is ready for a DMA transfer ($\overline{DACK} = \overline{CS}$ AND $A_0 = 0$)

DRQ [DMA Request]

This output signals that the μPD7720 is requesting a data transfer on the data bus.

P_0, P_1

These pins are general purpose output control lines.

D_0-D_7 [Data Bus]

This three-state I/O data bus transfers data between the data register or status register and the external data bus.

GND

This is the connection to ground.

CLK

This is the single-phase master clock input.

RST [Reset]

This input initializes the μPD7720 internal logic and sets the PC to 0.

INT [Interrupt]

A low to high transition on this pin executes a call instruction to location 100H, if interrupts were previously enabled.

SCK [Serial Data I/O Clock]

When this input is high, a serial data bit is transferred.

$\overline{SIEN}$ [Serial Input Enable]

This input enables the shift clock to the serial input register.

$\overline{SOEN}$ [Serial Output Enable]

This input enables the shift clock to the serial output register.

SI [Serial Data Input]

This pin inputs 8- or 16-bit serial data words from an external device such as an A/D converter.

SO [Serial Data Output]

This three-state port outputs 8- or 16-bit data words to an external device such as a D/A converter.

SORQ [Serial Data Output Request]

This output specifies to an external device that the serial data register has been loaded and is ready for output. SORQ is reset when the entire 8- or 16-bit word has been transferred.

$\overline{WR}$ [Write Control Signal]

This input writes data from the data port into the data register.

$\overline{RD}$ [Read Control Signal]

This input latches data from the data or status register to the data port where it is read by an external device.

$\overline{CS}$ [Chip Select]

This input enables data transfer through the data port with $\overline{RD}$ or $\overline{WR}$.

A_0 [Status Data Register Select]

This input selects data register for read/write (low) or status register for read (high).

V_{CC} [Power Supply]

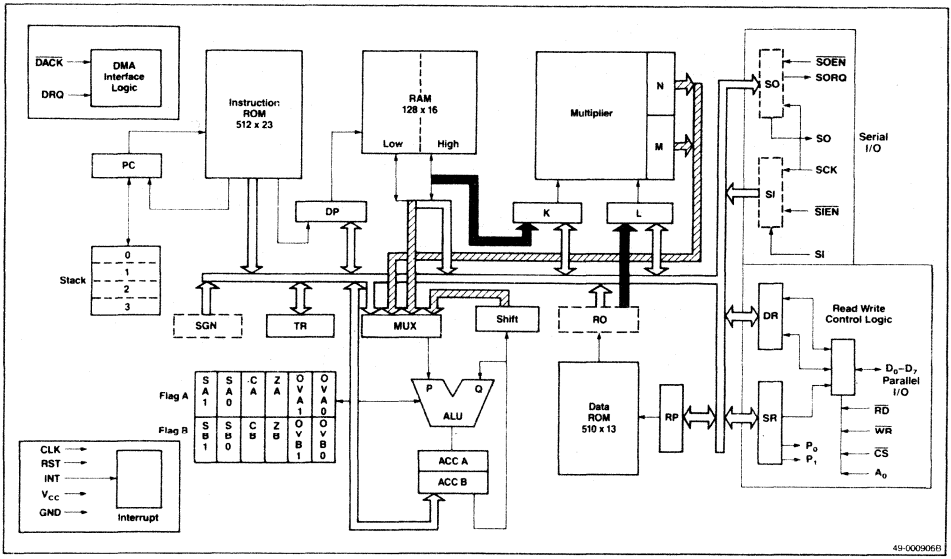
This pin is the +5 V power supply.

Functional Description

The primary bus (which is unshaded in the block diagram) makes a data path between all of the registers (including I/O), memory, and processing sections. This bus is referred to as the IDB (internal data bus). The multiplier input registers K and L can be loaded not only from the IDB but alternatively (via buses which are darkened in the block diagram) directly from RAM to the K register and directly from data ROM to the L register. Output from the multiplier in the M and N registers is typically added (via buses that are shaded in the block diagram) to either accumulator A or B as part of a multi-operation instruction.

Fabricated in high speed NMOS, the μPD7720A SPI is a complete 16-bit microcomputer on a single chip. ROM space provides program and coefficient storage; the on-chip RAM may be used for temporary data, coefficients, and results. A 16-bit arithmetic/logic unit (ALU) and a separate 16 x 16-bit fully parallel multiplier provide computational power. This combination allows the implementation of a "sum of products" operation in a single 250 ns instruction cycle. In addition, each arithmetic instruction allows a number of data movement operations to further increase throughput. Two serial I/O ports interface to codecs and other serially-oriented devices, while a parallel port provides both data and status information to conventional microprocessors. Handshaking signals, including DMA controls, allow the SPI to act as a sophisticated programmable peripheral as well as a stand-alone microcomputer.

Block Diagram



Memory

Memory is divided into three types: instruction ROM, data ROM, and data RAM. The 512 x 23-bit words of instruction ROM are addressed by a 9-bit program counter which can be modified by an external reset, interrupt, call, jump, or return instruction.

The data ROM is organized in 510 x 13-bit words which are addressed through a 9-bit ROM pointer (RP register). The RP may be modified simultaneously with arithmetic instructions so that the next value is available for the next instruction. The data ROM is ideal for storing the necessary coefficients, conversion tables, and other constants for your processing needs. Do not use data ROM locations 0 and 1 in the μPD7720A, where these locations are reserved for storage of test pattern data. (When submitting code for μPD7720A, these locations should be set to 0). Note that μPD77P20 allows use of these locations, but using them is not advised.

The data RAM is 128 x 16-bit words and is addressed through a 7-bit data pointer (DP register). The DP has extensive addressing features that operate simultaneously with arithmetic instructions, eliminating additional time for addressing or address modification.

Arithmetic Capabilities

One of the unique features of the SPI's architecture is its arithmetic facilities. With a separate multiplier, ALU, and multiple internal data paths, the SPI is capable of carrying out a multiply, an add or other arithmetic operation, and a data move between internal registers in a single instruction cycle.

ALU

The ALU is a 16-bit two's complement unit capable of executing 16 distinct operations on virtually any of the SPI's internal registers, thus giving the SPI both speed and versatility for efficient data management.

Accumulators [ACCA/ACCB]

Associated with the ALU are two 16-bit accumulators, each with its own set of flags, which are updated at the end of each arithmetic instruction (except NOP). Table 1 shows the ACC A/B flag registers. In addition to zero result, sign, carry, and overflow flags, the SPI incorporates auxiliary overflow and sign flags (SA1, SB1, OVA1, OVB1). These flags enable the detection of an overflow condition and maintain the correct sign after as many as three successive additions or subtractions.

Table 1. ACC A/B Flag Registers

Flag A	SA1	SA0	CA	ZA	OVA1	OVA0
Flag B	SB1	SB0	CB	ZB	OVB1	OVB0

Sign Register [SGN]

When OVA1 is set, the SA1 bit will hold the corrected sign of the overflow. The SGN register will use SA1 to automatically generate saturation constants 7FFFH(+) or 8000H(−) to permit efficient limiting of a calculated value. The SGN register is not affected by arithmetic operations on accumulator B, but flags SB1, SB0, CB, ZB, OVB1 and OVB0 are affected by accumulator B arithmetic operations.

Multiplier

Thirty-one bit results are developed by a 16 x 16-bit two's complement multiplier in 250 ns. The result is automatically latched to two 16-bit register M&N (sign and 15 higher bits in M, 15 lower bits in N; LSB in N is zero) at the end of each instruction cycle. A new product is available for use after every instruction cycle, providing significant advantages in maximizing processing speed for real-time signal processing.

Stack

The SPI contains a 4-level program stack for efficient program usage and interrupt handling.

Interrupt

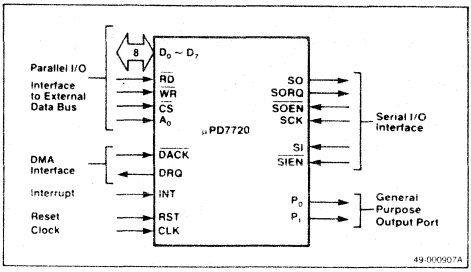
The SPI supports a single-level interrupt. Upon sensing a high level on the INT terminal, a subroutine call to location 100H is executed. The EI bit of the status register automatically resets to 0, disabling the interrupt facility until it is reenabled under program control.

Input/Output

General

The NEC SPI has three communication ports, as shown in figure 1: two serial and one 8-bit parallel, each with its own control lines for interface handshaking. Parallel port operation is software-configurable to be in either polled mode or DMA mode. A general purpose 2-line output port rounds out a full complement of interface capability.

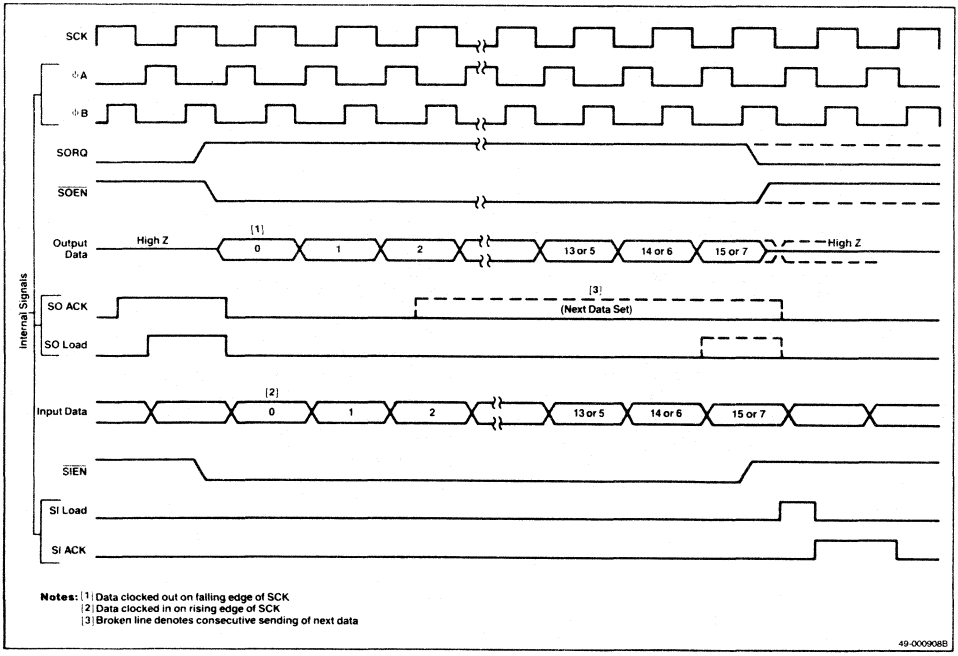
Figure 1. μPD7720A/μPD7720 Communication Ports



Serial I/O

The two shift registers (SI, SO) are software-configurable to single or double byte transfers. The shift registers are externally clocked (SCK) to provide a simple interface between the SPI and serial peripherals such as A/D and D/A converters, codecs, or other SPIs. Figure 2 shows serial I/O timing

Figure 2. Serial I/O Timing



Parallel I/O

The 8-bit parallel I/O port may be used for transferring data or reading the SPI's status, as shown in table 2. Data transfer is handled through a 16-bit data register (DR) that is software-configurable for double or single byte data transfers. The port is ideally suited for operating with 8080, 8085, and 8086 processor buses and may be used with other processors and computer systems.

Table 2. Parallel R/W Operation

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Operation
1	X	X	X	No effect on internal operation. D_0-D_7 are at high impedance levels.
X	X	1	1	
0	0	0	1	Data from D_0-D_7 is latched to DR (Note 1)
0	0	1	0	Contents of DR are output to D_0-D_7 (Note 1)
0	1	0	1	Illegal (SR is read only)
0	1	1	0	Eight MSBs of SR are output to D_0-D_7
0	X	0	0	Illegal (May not read and write simultaneously)

Note:

(1) Eight MSBs or 8 LSBs of data register (DR) are used, depending on DR status bit (DRS). The condition of $\overline{DACK}$ = 0 is equivalent to A_0 = CS = 0.

DMA Mode Option

Parallel data transfers may be controlled (optionally) via DMA control lines DRQ and $\overline{DACK}$. DMA mode allows high speed transfers and reduced processor overhead. When in DMA mode, $\overline{DACK}$ input resets DRQ output when data transfer is completed. $\overline{DACK}$ does not affect any status register bit or flag bit.

Status Register

The status register, shown in figure 3, is a 16-bit register in which the eight most significant bits may be read by the system's microprocessor for the latest parallel data I/O status. The RQM and DRS bits can only be affected by parallel data moves. The other bits can be written to (or read) by the SPI's load immediate (LDI) or move (MOV) instructions. The EI bit is automatically reset when an interrupt is serviced.

Figure 3. Status Register (SR)

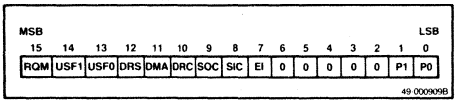


Table 3. Status Register Flags

Flag	Description
RQM (Request for Master)	A read or write from DR to IDB sets RQM = 1. An external read (write) resets RQM = 0.
USF1 and USF0 (User Flags 1 and 0)	General purpose flags which may be read by an external processor for user-defined signaling
DRS (DR Status)	For 16-bit DR transfers (DRC = 0). DRS = 1 after first 8 bits have been transferred. DRS = 0 after all 16 bits have been transferred.
DMA (DMA Enable)	DMA = 0 (Non-DMA transfer mode) DMA = 1 (DMA transfer mode)
DRC (DR control)	DRC = 0 (16-bit mode) DRC = 1 (8-bit mode)
SOC (SO Control)	SOC = 0 (16-bit mode) SOC = 1 (8-bit mode)
SIC (SI Control)	SIC = 0 (16-bit mode) SIC = 1 (8-bit mode)
EI (Enable Interrupt)	EI = 0 (interrupts disabled) EI = 1 (interrupts enabled)
P1, P0 (Ports 0 and 1)	P0 and P1 directly control the state of output pins P_0 and P_1

Instructions

The SPI has three types of instructions. Each of the three types take the form of a 23-bit word, and each executes in 250 ns.

Instruction Timing

To control the execution of instructions, the external 8 MHz clock is divided into four phases for internal execution. The various elements of the 23-bit instruction word are executed in a set order. Multiplication automatically begins first. Also, data moves from source to destination before other elements of the instruction. Data being moved on the internal data bus (IDB) is available for use in ALU operations (if P-select field of the instruction specifies IDB). However, if the accumulator specified in the ASL field is also specified as the destination of the data move, the ALU operation becomes a NOP, as the data move supersedes the ALU operation.

Pointer modifications occur at the end of the instruction cycle — after their values have been used for data moves. The result of multiplication is available at the end of the instruction cycle for possible use in the next instruction. If a return is specified as part of an OP instruction, it is executed last.

An assembly language 'OP' instruction may consist of what looks like one to six lines of assembly code, but all of these lines are assembled together into one 23-bit instruction word. Therefore, the order of the six lines makes no difference in the order of execution described above. However, for understanding the SPI's operation and to eliminate confusion, write assembly code in the order described; that is: data move, ALU operations, data pointer modifications, then return.

OP/RT Instruction Field Specification

Figure 4 illustrates the OP/RT instruction field specification. There are two instructions of this type, both of which are capable of executing all ALU functions listed in table 5. The ALU functions operate on the value specified by the P-select field (see table 4).

Besides the arithmetic functions, these instructions can also (1) modify the RAM data pointer DP, (2) modify the data ROM pointer RP, and (3) move data along the on-chip data bus from a source register to a destination register (the possible source and destination registers are listed in tables 10 and 11, respectively). The difference in the two instructions of this type is that RT executes a subroutine or interrupt return at the end of the instruction cycle, but the OP does not. Tables 6, 7, 8, and 9 show the ASL, DPL, DPH and RPDCR fields, respectively.

Figure 4. OP/RT Instruction Field

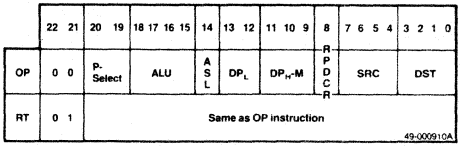


Table 4. P-Select Field

Mnemonic	D_{20}	D_{19}	ALU Input
RAM	0	0	RAM
IDB	0	1	Internal Data Bus (Note 1)
M	1	0	M Register
N	1	1	N Register

Note:

(1) Any value on the on-chip data bus. Value may be selected from any of the registers listed in table 6 source register selections.

Table 5. ALU Field

Mnemonic	D_{18}	D_{17}	D_{16}	D_{15}	ALU Function	SA1 SB1	SA0 SB0	CA CB	ZA ZB	OVA1 OVB1	OVA0 OVB0
NOP	0	0	0	0	No operation	—	—	—	—	—	—
OR	0	0	0	1	OR	x	Δ	0	Δ	0	0
AND	0	0	1	0	AND	x	Δ	0	Δ	0	0
XOR	0	0	1	1	Exclusive OR	x	Δ	0	Δ	0	0
SUB	0	1	0	0	Subtract	Δ	Δ	Δ	Δ	Δ	Δ
ADD	0	1	0	1	ADD	Δ	Δ	Δ	Δ	Δ	Δ
SBB	0	1	1	0	Subtract with borrow	Δ	Δ	Δ	Δ	Δ	Δ
ADC	0	1	1	1	Add with carry	Δ	Δ	Δ	Δ	Δ	Δ
DEC	1	0	0	0	Decrement ACC	Δ	Δ	Δ	Δ	Δ	Δ
INC	1	0	0	1	Increment ACC	Δ	Δ	Δ	Δ	Δ	Δ
CMP	1	0	1	0	Complement ACC (one's complement)	x	Δ	0	Δ	0	0
SHR1	1	0	1	1	1-Bit right shift	x	Δ	Δ	Δ	0	0
SHL1	1	1	0	0	1-Bit left shift	x	Δ	Δ	Δ	0	0
SHL2	1	1	0	1	2-Bit left shift	x	Δ	0	Δ	0	0
SHL4	1	1	1	0	4-Bit left shift	x	Δ	0	Δ	0	0
XCHG	1	1	1	1	8-Bit exchange	x	Δ	0	Δ	0	0

Note:

Δ May be affected, depending on the results
— Previous status can be held
0 Reset
x Indefinite

Table 6. ASL Field

Mnemonic	D_{14}	ACC Selection
ACCA	0	ACCA
ACCB	1	ACCB

Table 7. DPL Field

Mnemonic	D_{13}	D_{12}	Low DP Modify (DP_3-DP_0)
DPNOP	0	0	No operation
DPINC	0	1	Increment DPL
DPDEC	1	0	Decrement DPL
DPCLR	1	1	Clear DPL

Table 8. DPH Field

Mnemonic	D_{11}	D_{10}	D_9	High DP Modify
M0	0	0	0	Exclusive OR of DPH (DP_6-DP_4) with the mask defined by the three bits (D_{11}-D_9) of the DPH field
M1	0	0	1	
M2	0	1	0	
M3	0	1	1	
M4	1	0	0	
M5	1	0	1	
M6	1	1	0	
M7	1	1	1	

Table 9. RPDCR Field

Mnemonic	D_8	RP Operation
RPNOP	0	No operation
RPDEC	1	Decrement RP

Table 10. SRC Field

Mnemonic	D_7	D_6	D_5	D_4	Source Register
NON	0	0	0	0	No register
A	0	0	0	1	ACCA (Accumulator A)
B	0	0	1	0	ACCB (Accumulator B)
TR	0	0	1	1	TR temporary register
DP	0	1	0	0	DP data pointer
RP	0	1	0	1	RP ROM pointer
RO	0	1	1	0	RO ROM output data
SGN	0	1	1	1	SGN sign register

Table 10. SRC Field (cont)

Mnemonic	D_7	D_6	D_5	D_4	Source Register
DR	1	0	0	0	DR data register
DRNF	1	0	0	1	DR no flag (Note 1)
SR	1	0	1	0	SR status register
SIM	1	0	1	1	SI serial in MSB (Note 2)
SIL	1	1	0	0	SI serial in LSB (Note 3)
K	1	1	0	1	K register
L	1	1	1	0	L register
MEM	1	1	1	1	RAM

Note:

(1) DR to IDB, RQM not set. In DMA, DRQ not set.

(2) First bit in goes to MSB, last bit to LSB.

(3) First bit goes to LSB, last bit to MSB (bit reversed).

Table 11. DST Field

Mnemonic	D_3	D_2	D_1	D_0	Destination Register
@NON	0	0	0	0	No register
@A	0	0	0	1	ACCA (Accumulator A)
@B	0	0	1	0	ACCB (Accumulator B)
@TR	0	0	1	1	TR temporary register
@DP	0	1	0	0	DP data pointer
@RP	0	1	0	1	RP ROM pointer
@DR	0	1	1	0	DR data register
@SR	0	1	1	1	SR status register
@SOL	1	0	0	0	SO serial out LSB (Note 1)
@SOM	1	0	0	1	SO serial out MSB (Note 2)
@K	1	0	1	0	K (Mult)
@KLR	1	0	1	1	IDB → K, ROM → L (Note 3)
@KLM	1	1	0	0	Hi RAM → K, IDB → L (Note 4)
@L	1	1	0	1	L (Mult)
@NON	1	1	1	0	No register
@MEM	1	1	1	1	RAM

Note:

(1) LSB is first bit out.

(2) MSB is first bit out.

(3) Internal data bus to K, and ROM to L register.

(4) Contents of RAM address specified by $DP_6 = 1$, is placed in K register, IDB is placed in L (that is, 1, DP_5, DP_4 DP_3-DP_0).

Jump/Call/Branch

Figure 5 shows the JP instruction field specification.

Three types of program counter modifications are accommodated by the processor and are listed in table 12. All the instructions, if unconditional or if the specified condition is true, take their next program execution address from the next address field (NA); otherwise PC = PC + 1.

Table 12. BRCH Field

D_{20}	D_{19}	D_{18}	Branch Instruction
1	0	0	Unconditional jump
1	0	1	Subroutine call
0	1	0	Conditional jump

For the conditional jump instruction, the condition field specifies the jump condition. Table 13 lists all the instruction mnemonics of the jump/call/branch codes.

Load Data [LDI]

Figure 6 shows the LD instruction field specification.

The load data instruction will take the 16-bit value contained in the immediate data field (ID) and place it in the location specified by the destination field (DST) (see table 11).

Figure 5. JP Instruction Field Specification

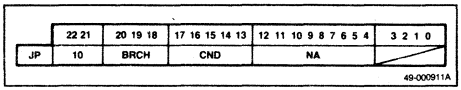


Figure 6. LD Instruction Field Specification

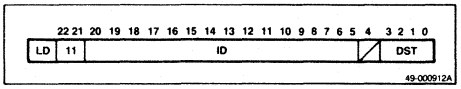


Table 13. BRCH/CND Fields

Mnemonic	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	Conditions (Note 1)
JMP	1	0	0	0	0	0	0	0	No condition
CALL	1	0	1	0	0	0	0	0	No condition
JNCA	0	1	0	0	0	0	0	0	CA = 0
JCA	0	1	0	0	0	0	0	1	CA = 1
JNCB	0	1	0	0	0	0	1	0	CB = 1
JCB	0	1	0	0	0	0	1	1	CB = 1
JNZA	0	1	0	0	0	1	0	0	ZA = 0
JZA	0	1	0	0	0	1	0	1	ZA = 1
JNZB	0	1	0	0	0	1	1	0	ZB = 0
JZB	0	1	0	0	0	1	1	1	ZB = 1
JNOVA0	0	1	0	0	1	0	0	0	OVA0 = 0
JOVA0	0	1	0	0	1	0	0	1	OVA0 = 1
JNOVB0	0	1	0	0	1	0	1	0	OVB0 = 0
JOVB0	0	1	0	0	1	0	1	1	OVB0 = 1
JNOVA1	0	1	0	0	1	1	0	0	OVA1 = 0
JOVA1	0	1	0	0	1	1	0	1	OVA1 = 1
JNOVB1	0	1	0	0	1	1	1	0	OVB1 = 0
JOVB1	0	1	0	0	1	1	1	1	OVB1 = 1
JNSA0	0	1	0	1	0	0	0	0	SA0 = 0
JSA0	0	1	0	1	0	0	0	1	SA0 = 1
JNSB0	0	1	0	1	0	0	1	0	SB0 = 0
JSB0	0	1	0	1	0	0	1	1	SB0 = 1
JNSA1	0	1	0	1	0	1	0	0	SA1 = 0
JSA1	0	1	0	1	0	1	0	1	SA1 = 1
JNSB1	0	1	0	1	0	1	1	0	SB1 = 0
JSB1	0	1	0	1	0	1	1	1	SB1 = 1
JDPL0	0	1	0	1	1	0	0	0	DPL = 0
JDPLF	0	1	0	1	1	0	0	1	DPL = FH
JNSIAK	0	1	0	1	1	0	1	0	SI ACK = 0
JSIAK	0	1	0	1	1	0	1	1	SI ACK = 1
JNSOAK	0	1	0	1	1	1	0	0	SO ACK = 0
JSOAK	0	1	0	1	1	1	0	1	SO ACK = 1
JNRQM	0	1	0	1	1	1	1	0	RQM = 0
JRQM	0	1	0	1	1	1	1	1	RQM = 1

Note:

(1) BRCH or CND values not in this table are prohibited.

μPD7720A, μPD77P20

Absolute Maximum Ratings

Supply voltage, V_{CC} (7720A)	−0.5 to +7.0 V
Supply voltage, V_{CC} (77P20)	−0.3 to +7.0 V
Programming voltage, V_{PP} (77P20 only)	−0.3 to +22 V
Input voltage, V_I (7720A)	−0.5 to +7.0 V
Input voltage, V_I (77P20)	−0.3 to +7.0 V
Output voltage, V_O (7720A)	−0.5 to +7.0 V
Output voltage, V_O (77P20)	−0.3 V to +7.0 V
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5$ V ±5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5		0.8	V	
Input high voltage	V_{IH}	2.0		$V_{CC}+0.5$	V	
CLK low voltage	$V_{\phi L}$	−0.5		0.45	V	
CLK high voltage	$V_{\phi H}$	3.5		$V_{CC}+0.5$	V	
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -400\ \mu$A
Input load current	I_{LIL}			−10	μA	$V_{IN} = 0$ V
Input load current	I_{LIH}			10	μA	$V_{IN} = V_{CC}$
Output float leakage	I_{LOL}			−10	μA	$V_{OUT} = 0.47$ V
Output float leakage	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
Power supply current (7720A)	I_{CC}		120	170	mA	
Power supply current (77P20)	I_{CC}		270	350	mA	
V_{PP} current (77P20 only)	I_{PP}			70	mA	Program mode max pulse current (Note 1)
		0.5		3.0	mA	Program verify, inhibit (Note 2)

Note:

(1) $V_{PP} = 21 \pm 0.5$ V

(2) For K-level parts, V_{PP} max = $(V_{CC} - 0.6\text{ V}) + 0.25$ V
V_{PP} min = $(V_{CC} - 0.6\text{ V}) - 0.25$ V
For all other step levels: V_{PP} max = $V_{CC} + 0.25$ V
V_{PP} min = $V_{CC} - 0.85$ V

Capacitance

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
CLK, SCK capacitance	C_ϕ		20	pF	$f_c = 1$ MHz
Input pin capacitance	C_{IN}		10	pF	
Output pin capacitance	C_{OUT}		20	pF	

AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5$ V ±5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK cycle time μPD7720A	ϕ_{CY}	120		2000	ns	(Note 1)
CLK cycle time μPD77P20	ϕ_{CY}	122		2000	ns	(Note 1)
CLK pulse width	ϕ_D	60			ns	(Note 4)
CLK rise time	ϕ_R			10	ns	(Note 1)
CLK fall time	ϕ_F			10	ns	(Note 1)
Address setup time for $\overline{RD}$	t_{AR}	0			ns	
Address hold time for $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ pulse width	t_{RR}	250			ns	
Data delay from $\overline{RD}$	t_{RD}			150	ns	$C_L = 100$ pF
Read to data floating	t_{DF}	10		100	ns	$C_L = 100$ pF
Address setup time for $\overline{WR}$	t_{AW}	0			ns	
Address hold time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ pulse width	t_{WW}	250			ns	
Data setup time for $\overline{WR}$	t_{DW}	150			ns	
Data hold time for $\overline{WR}$	t_{WD}	0			ns	
$\overline{RD}$, $\overline{WR}$, recovery time	t_{RV}	250			ns	(Note 2)
DRQ delay	t_{AM}			150	ns	
$\overline{DACK}$ delay time	t_{DACK}	1			ϕD	(Note 2)
$\overline{DACK}$ pulse width	t_{DD}	250		2000	μs	μPD7720A
		250		50000	μs	μPD77P20
SCK cycle time	t_{SCY}	480		DC	ns	
SCK pulse width	t_{SCK}	230			ns	
SCK rise/fall time	t_{RSC}/t_{FSC}			20	ns	
SORQ delay	t_{DRQ}	30		150	ns	$C_L = 100$ pF
$\overline{SOEN}$ setup time	t_{SOC}	50			ns	
$\overline{SOEN}$ hold time	t_{CSO}	30			ns	

μPD7720A, μPD77P20

AC Characteristics (cont)

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5\ V \pm 5\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
SO delay from SCK = low	t_{DCK}			150	ns	
SO delay from SCK before 1st bit (Note 3)	t_{DZRQ}	20		300	ns	(Note 2)
SO delay from SCK	t_{DZSC}	20		300	ns	(Note 2)
SO delay for $\overline{SOEN}$	t_{DZE}	20		180	ns	(Note 2)
$\overline{SOEN}$ to SO floating	t_{HZE}	20		200	ns	(Note 2)
SCK to SO floating with SORQ high	t_{HZSC}	20		300	ns	(Note 2)
SO delay from SCK for last bit	t_{HZRQ}	70		300	ns	(Note 2)
$\overline{SIEN}$, SI setup time	t_{DC}	55			ns	(Note 2)
$\overline{SIEN}$, SI hold time	t_{CD}	30			ns	
P_0, P_1 delay	t_{DP}			ϕ_{CY} +150	ns	
RST pulse width	t_{RST}	4			ϕ_{CY}	
INT pulse width	t_{INT}	8			ϕ_{CY}	

Notes:

(1) Voltage at timing measuring point: 1.0 V and 3.0 V.

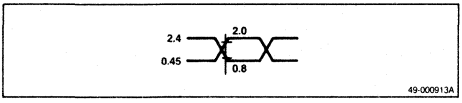
(2) Voltage at AC timing measuring point:
$V_{IL} = V_{OL} = 0.8\ V$
$V_{IH} = V_{OH} = 2.0\ V$

(3) SO goes out of tristate, but data is not valid yet.

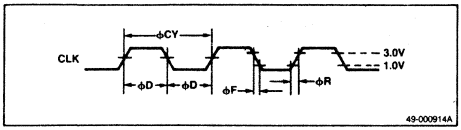
(4) Pulse width includes CLK rise and fall times. Refer to Clock Timing Waveform.

Timing Waveforms

Input Waveform of AC Test (except CLK)

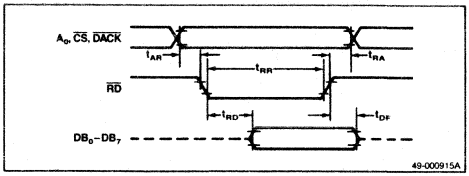


Clock

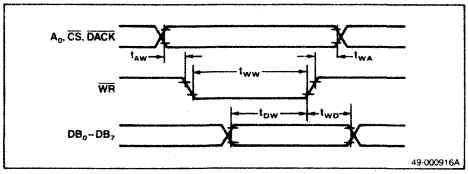


Timing Waveforms (cont)

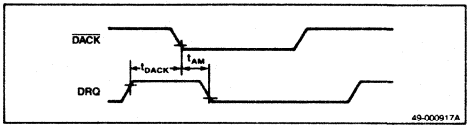
Read Operation



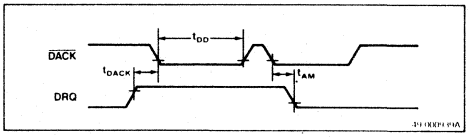
Write Operation



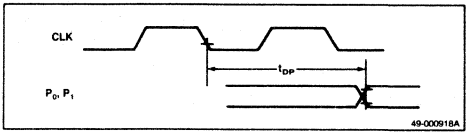
DMA Operation



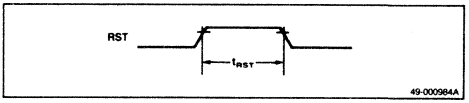
16 Bit Transfer Mode



Port Output

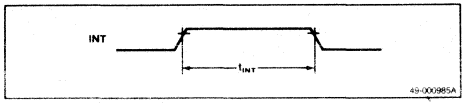


Reset



Timing Waveforms (cont)

Interrupt



Serial Timing

Figure 7 shows serial output timing when $\overline{SOEN}$ is asserted in response to SORQ when SCK is low. If $\overline{SOEN}$ is held inactive until after SORQ is asserted, and then $\overline{SOEN}$ is asserted while SCK is low ($\overline{SOEN}$ should be held inactive until the period of t_{CSO}, after the falling edge of SCK), SO will become active but not valid t_{DZSC} after the next rising edge of SCK. SO will become valid with the first bit t_{DCK} after the next falling edge of SCK, for use by an external device at the subsequent rising edge of SCK. Subsequent bits will be shifted out t_{DCK} after subsequent falling edges of SCK, for use at subsequent rising edges of SCK. The last bit to be shifted out will also follow this pattern, and will be held valid t_{HZRQ} after the corresponding rising edge of SCK at which it is to be used. SORQ will be held t_{DRQ} after this same rising edge of SCK, then removed. $\overline{SOEN}$ should be released at least t_{SOC} before the next falling edge of SCK.

Figure 8 shows timing for serial output when $\overline{SOEN}$ is asserted in response to SORQ when SCK is high. If $\overline{SOEN}$ is held inactive until after SORQ is asserted, and then $\overline{SOEN}$ is asserted while SCK is high (at least t_{SOC} before the falling edge of SCK), SO will become active but not valid t_{DZE} after the falling edge of $\overline{SOEN}$. SO will become valid t_{DCK} after the falling edge of SCK, for use by an external device at the subsequent rising edge of SCK. Note that, although figure 8 shows $\overline{SOEN}$ being asserted during a different SCK pulse than the one in which SORQ is asserted, it is permissible for these to occur during the same pulse of SCK, as long as $\overline{SOEN}$ is still asserted t_{SOC} before the falling edge of SCK. The timing for the second through the last bits is identical to the timing shown in figure 7.

Figure 9 shows output timing when $\overline{SOEN}$ is active before SORQ is high. If $\overline{SOEN}$ is held active before SORQ is high, data will be shifted out whenever it becomes available in the serial output register (assuming previous data is already shifted out). In this case, SORQ will rise t_{DRQ} after a rising edge of SCK. SO will become active (but not valid yet) t_{DZRQ} after the same rising edge of SCK. The first valid SO bit occur t_{DCK} after the next falling edge of SCK, for use by an external device at the subsequent rising edge of SCK. Subsequent bits will be shifted out t_{DCK} after subsequent falling edges of SCK, for use at subsequent rising edges of SCK. The last bit to be shifted out will also follow this pattern, and will be held valid t_{HZRQ} after the corresponding rising edge of SCK at which it is to be used. SORQ will be held t_{DRQ} after this same rising edge of SCK, then removed.

Avoid releasing $\overline{SOEN}$ in the middle of a transfer (that is, before the last bit is shifted out), since this will stop the output shift operation, and, when $\overline{SOEN}$ is again asserted, the remainder of the transfer will be shifted out before the next transfer can begin. The next tranfer will begin immediately without any indication of the byte/word boundary. If $\overline{SOEN}$ is released while SCK is high, as shown in figure 10, at least t_{SOC} before the falling edge of SCK, then SO will go inactive t_{HZE} after $\overline{SOEN}$ is released (which may be before or after the falling edge of SCK).

If $\overline{SOEN}$ is released while SCK is low, as in figure 11, at least t_{CSO} after the falling edge of SCK, then the next bit will be shifted out t_{DCK} after the falling edge of SCK, for use at the subsequent rising edge of SCK. SO will then go inactive t_{HZSC} after this rising edge of SCK.

Note:

For all its uses, $\overline{SOEN}$ must not change state within t_{SOC} before or t_{CSO} after the falling edge of SCK; otherwise, the results will be indeterminate.

Serial input timing, shown in figure 12, is much simpler than serial output timing. Data bits are shifted in on the rising edge of SCK if $\overline{SIEN}$ is asserted. Both $\overline{SIEN}$ and SI must be stable at least t_{DC} before and t_{CD} after the rising edge of SCK; otherwise the results will be indeterminate.

Figure 13 shows serial timing of cascaded SPIs with a common SCK. SO from the first SPI equals SI of the second, and the first SPI's SORQ inverts to become $\overline{SIEN}$ of the second. $\overline{SOEN}$ of the first SPI is always asserted.

Figure 7. Serial Output Case #1: $\overline{SOEN}$ Asserted in Response to SORQ when SCK is Low

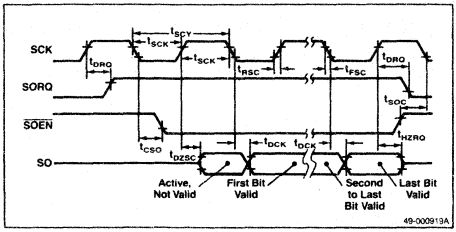


Figure 8. Serial Output Case #2: $\overline{SOEN}$ Asserted in Response to SORQ when SCK is High

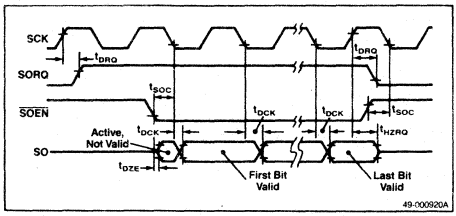


Figure 9. Serial Output Case #3: $\overline{SOEN}$ Active before SORQ is High

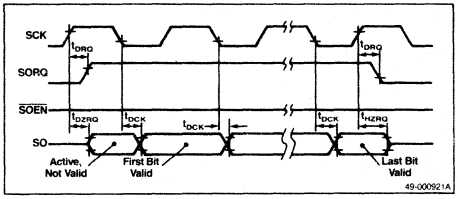


Figure 10. Serial Output Case #4A: If $\overline{SOEN}$ is Released in the Middle of a Transfer During SCK High

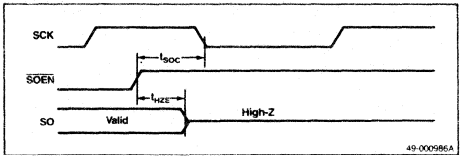


Figure 11. Serial Output Case #4B: If $\overline{SOEN}$ is Released in the Middle of a Transfer During SCK Low.

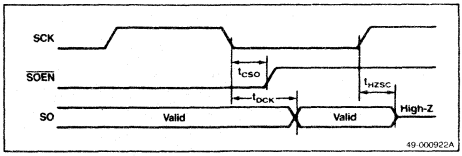


Figure 12. Serial Input

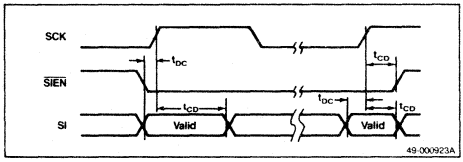
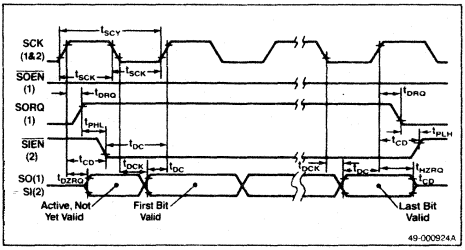


Figure 13. Serial Timing Example



When cascading two SPIs in the described configuration, most of the timing involved is directly copied from the case of serial output with $\overline{SOEN}$ always enabled (figure 13). It must be shown that the results will be suitable for the serial input timing of the second SPI.

(1) SORQ (1) rises t_{DRQ} after a rising edge of SCK, and it is inverted (inverter has t_{PHL} delay time) to become $\overline{SIEN}$ (2), which must be stable t_{DC} before the next rising edge of SCK. It also must not change until t_{CD} after this first rising edge of SCK, as shown by case 2 in figure 8.

$$t_{DRQ}(max) + t_{PHL} + t_{DC}(min) \leq t_{SCY}(min)$$
$$t_{PHL}(max) \leq t_{SCY}(min) - t_{DC}(min) - t_{DRQ}(max)$$
$$\leq 480 - 55 - 150$$
$$\leq 275 \text{ nsec—readily achieved by 74LS14, for example}$$

(2) SORQ (1) is released t_{DRQ} after the last useful rising edge of SCK, and is inverted (inverter has t_{PHL} delay time) to become $\overline{SIEN}$ (2), which must remain stable t_{CD} after the rising edge of SCK.

$$t_{DRQ}(min) + t_{PLH}(min) \geq t_{CD}(min)$$
$$t_{PLH}(min) \geq t_{CD}(min) - t_{DRQ}(min)$$
$$\geq 30 - 30$$
$$\geq 0\text{—no problem, assuming causality}$$

Note:

This also shows $t_{PHL}(min) \geq 0$ for the rising edge of SORQ.

(3) SO (1) is valid t_{DCK} after a falling edge of SCK; since it becomes SI (2), it must be valid t_{DC} before the next rising edge of SCK.

$$t_{DCK}(max) + t_{DC}(min) \leq t_{SCK}(min)$$
$$150 + 55 \leq 230$$
$$205 \leq 230\text{—this condition is satisfied}$$

(4) SO (1) remains valid t_{HZRQ} after the last useful rising edge of SCK; since it becomes SI (2), it must remain valid t_{CD} after this rising edge of SCK.

$$t_{HZRQ}(min) \geq t_{CD}(min)$$
$$70 \geq 30\text{—this condition is satisfied}$$

Note:

The above calculations may need to be adjusted for rise and fall times, since t_{SCY} and t_{SCK} are measured for midpoints of wave slopes.

μPD77P20 UV Erasable EPROM Version

Function

The μPD77P20 operates from a single +5 V power supply and can accordingly be used in any μPD7720A masked ROM application.

Use of Evakit-7720

The following sections describe electrical conditions that are required for programming the μPD77P20. However, the Evakit-7720, NEC's hardware emulator development tool for the μPD7720A/μPD77P20, meets the electrical and timing specifications presented below. When the Evakit-7720 is used for programming μPD77P20, all data transfers and formatting are handled automatically by Evakit's monitor program. Please refer to the Evakit-7720(B) User's Manual for programing procedures.

The information presented below in the sections on Configuration, Operation, and Programming (and the various subsections) is required only for users who do NOT intend to use an Evakit to program the μPD77P20.

Configuration

Data transfer for programming and reading the internal ROM is partitioned into three bytes for each 23-bit wide instruction location and into two bytes for each 13-bit wide data location. Partitioning of data transfer into and out of the data port is shown in figure 14.

Instruction ROM

The instruction ROM data is transferred through the data port as a high byte, middle byte, and low byte as shown in figure 15. Bit 7 of the middle byte should be assigned a value of zero. Data is presented to the data port in a bit-reversed format. The LSB through the MSB of an instruction ROM byte is applied to the MSB through the LSB of the data port, respectively.

Data ROM

Figure 16 shows the data ROM format. The data ROM data is transferred through the data port as a low byte and a high byte as shown in figure 17. Bits 0, 1, and 2 of the low byte should be assigned a value of zero. Data is presented to the data port in corresponding order. The MSB through the LSB of a data ROM byte is applied to the MSB through the LSB of the data port, respectively.

Initially and after each erasure, all bits of the μPD77P20 are in the zero state.

Figure 14. Instruction ROM Format

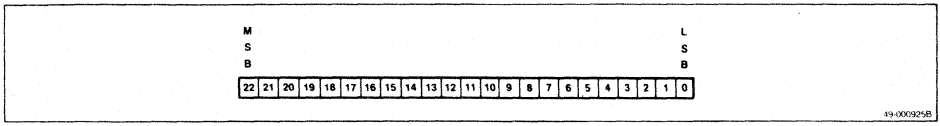


Figure 15. Transfer of Instruction ROM Data

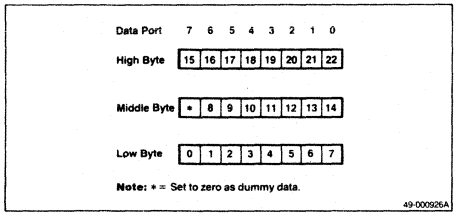


Figure 16. Data ROM Format

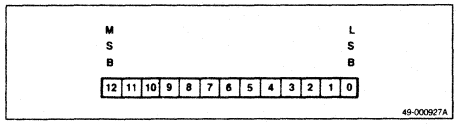
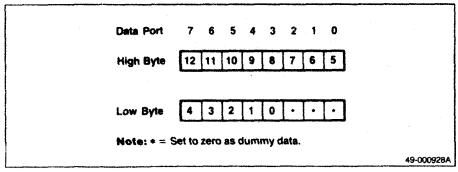


Figure 17. Transfer of Data ROM Data



Operating Modes

In order to read or write the instruction or data ROMs, the mode of operation of the μPD77P20 must be initially set. At the RST trailing edge, the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ should be logical zero and the $\overline{DACK}$, A_0, and SI signals should be set to determine the mode of operation accordingly, as set out in table 14.

Table 14. μPD77P20 Operation Mode

$\overline{DACK}$	A_0	SI	
0	0	0	Write mode instruction and data ROM
0	0	1	Read the instruction ROM
0	1	0	Read the data ROM

Once set, the μPD77P20 will remain in the selected mode. A reset is required to transfer to another mode.

Write Mode

The individual instruction ROM and data ROM bytes are specified by control signals $\overline{RD}$, A_0, SI, and INT as set out in table 15. Before writing the EPROM location, the bytes should be loaded accordingly.

Table 15. Write Mode Specification of ROM bytes

$\overline{RD}$	A_0	SI	INT	
1	0	0	1	Write instruction byte, high
1	0	1	0	Write instruction byte, middle
1	0	1	1	Write instruction byte, low
1	1	0	0	Write data byte, low
1	1	0	1	Write data byte, high

Read Mode

The instruction ROM and data ROM bytes are specified by the control signals $\overline{RD}$, A_0, SI, and INT as set out in table 16. Reading is accomplished by setting the control signals accordingly.

Table 16. Read Mode Specification of ROM Bytes

$\overline{RD}$	A0	SI	INT	
0	0	0	1	Read instruction byte, high
0	0	1	0	Read instruction byte, middle
0	0	1	1	Read instruction byte, low
1	0	0	0	Read data byte, high and low

The instruction ROM and data ROM are addressed by the 9-bit program counter and the 9-bit ROM pointer respectively. The PC is reset to 000H and is automatically incremented to the end address 1FFH. The RP is reset to 1FFH and is automaticaly decremented to 000H.

Erasing

Programming can only occur when all data bits are in an erased or low (0) level state. Erase μPD77P20 programmed data by exposing it to light with wavelengths shorter than approximately 4,000 angstroms. Note that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD77P20. Consequently, if the μPD77P20 will be exposed to these types of lighting conditions for long periods of time, mask its window to prevent unintentional erasure.

The recommended erasure procedure for the μPD77P20 is exposure to ultraviolet light with wavelengths of 2,537 angstroms. The integrated dose (i.e., UV intensity x exposure time) for erasure should not be less than 15 W-sec/cm^2. The erasure time is approximately 20 minutes using an ultraviolet lamp with a power rating of 12,000 μW/cm^2.

During erasure, place the μPD77P20 within one inch of the lamp tubes. If the lamp tubes have filters, remove the filters before erasure.

Programming

Programming of the μPD77P20 is achieved with a single 50 ms TTL pulse. Total programming time for the 11,776 bits of instruction EPROM and also for the 6,630 bits of data EPROM is 26 seconds. Data is entered by programming a high (1) level in the chosen bit locations. Both instruction ROM and data ROM should be programmed since they cannot be erased independently. Both instruction ROM and data ROM programming modes are entered in the same manner. The device must be reset initially before it can be placed into the programming mode. After being reset, the $\overline{WR}$ signal and all other inputs ($\overline{RD}$, $\overline{CS}$/PROG, $\overline{DACK}$, A_0, SI, and INT) should be a TTL low (0) signal t_{RS} prior to the falling edge of RST. $\overline{WR}$ is then held for t_{RH} before being set to a TTL high (1) level signal. The device is now in a programming mode and will stay in this mode, allowing ROM locations to be sequentially programmed.

Programming Mode—Instruction ROM. Instruction ROM locations are sequentially programmed from address 000H to address 1FFH. The location address is incremented by the application of CLK for a duration of t_{CY}. Data bytes for each location as specified by control signals $\overline{RD}$, A_0, SI, and INT (table 15) are clocked into the device by the falling edge of $\overline{RD}$. After the three bytes have been loaded into the device, V_{PP} is raised to 21 V ±0.5 V, t_{VS} prior to $\overline{CS}$/PROG transitioning to a TTL high (1) level signal. V_{PP} is held for the duration of t_{PRPR} plus t_{PRV} before returning to the V_{CC} level. After t_{PRCL} the instruction ROM address can be incremented to program the next location. Figure 18 shows the programming mode of instruction ROM timing.

Programming Mode—Data ROM. Data ROM locations are sequentially programmed from address 1FFH to address 000H. The location address is decremented by the application of CLK for t_{CY}. The data bytes for each location as specified by control signals $\overline{RD}$, A_0, SI, and INT are clocked into the device by the falling edge of $\overline{RD}$. After the two bytes have been loaded into the device, V_{PP} is raised to 21 V ±0.5 V, t_{VPR} prior to $\overline{CS}$/PROG transitioning to a TTL high (1) level signal. V_{PP} is held for the duration of t_{PRPR} plus t_{PRV} before returning to the V_{CC} level. After t_{PRCL} the data ROM address can be decremented to program the next location. Figure 19 shows programming mode of data ROM timing.

Read Mode. A read should be performed to verify that the data was programmed correctly. Prior to entering read mode the device must be reset.

Figure 18. Programming Mode of Instruction ROM

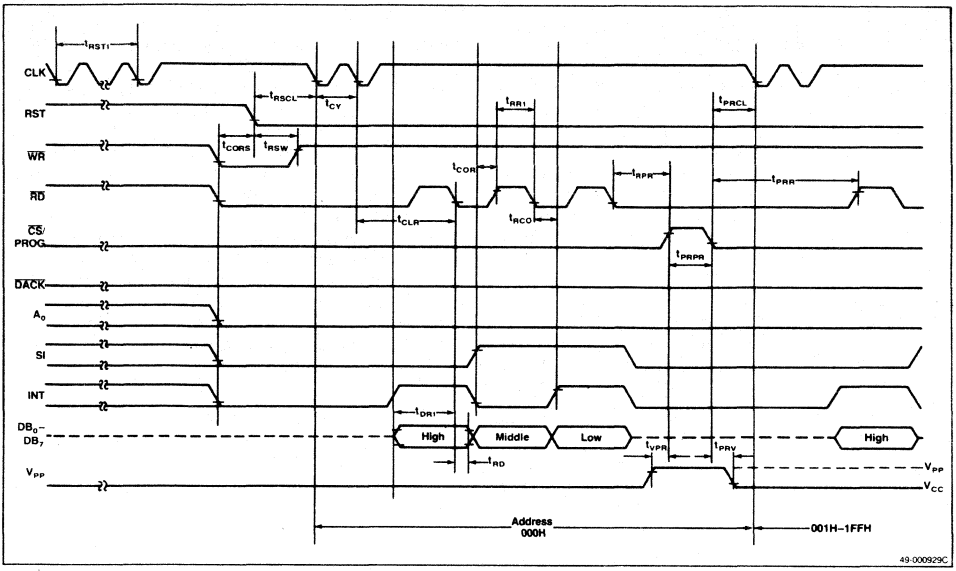
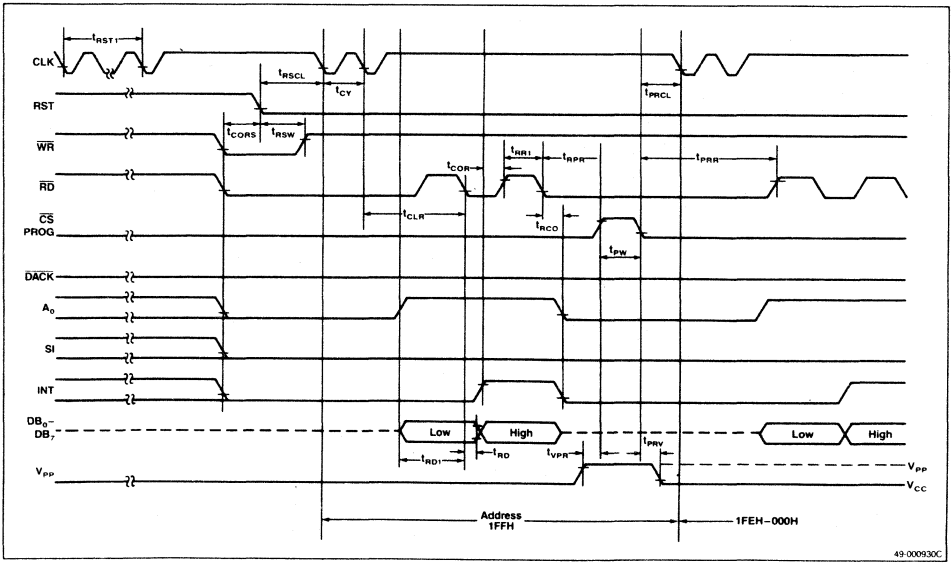


Figure 19. Programming Mode of Data ROM



Read Mode—Instruction ROM. This mode is entered by holding the $\overline{WR}$ signal at a TTL low (0) level with the SI signal at a TTL high (1) level and all other specified inputs ($\overline{RD}$, $\overline{CS}$/PROG, $\overline{DACK}$, A_0, INT) at TTL low (0) levels for t_{CORS} prior to the falling edge of RST. $\overline{WR}$ is then held for t_{RSW} before being set to a TTL high (1) level. The device is now in the instruction ROM read mode and will stay in this mode until reset. Instruction ROM locations are sequentially read from address 000H through 1FFH. Application of CLK for t_{CY} will increment the location address. The three data bytes will be read as specified by the control signals $\overline{RD}$, A_0, SI and INT (table 16). Figure 20 shows read mode of instruction ROM timing.

μPD77P20 Mode Selection

Mode	$\overline{CS}$/PROG	V_{PP}	V_{CC}	Outputs
Instruction ROM program	V_{IH}	V_{PP}	+5 V	D_{IN}
Data ROM program	V_{IH}	V_{PP}	+5 V	D_{IN}
Instruction ROM read	V_{IL}	V_{CC}	+5 V	D_{OUT}
Data ROM read operation	V_{IL}	V_{CC}	+5 V	D_{OUT},
	V_{IH}	V_{CC}	+5 V	D_{IN}, High Z

Read Mode—Data ROM. Figure 21 shows read mode of data ROM timing. This mode is entered by holding the $\overline{WR}$ signal at a TTL low (0) level with the A_0 signal at a TTL high (1) level and all other specified inputs ($\overline{RD}$, $\overline{CS}$/PROG, $\overline{DACK}$, SI, INT) at TTL low (0) levels for t_{CORS} prior to the falling edge of RST. $\overline{WR}$ and A_0 are then held for t_{RSW} prior to the falling edge of RST. $\overline{WR}$ and A_0 are then held for t_{RSW} before being set to a TTL high (1) level and TTL low (0) level, respectively. The device is now in the data ROM read mode and will stay in this mode until it is reset. Data ROM locations are sequentially read from address 1FFH through 000H. Application of CLK for t_{CY} will decrement the location address. After decrementing the location address, the low byte of the current location will be available at the data port subsequent to a t_{CLD} delay. Application of $\overline{RD}$ will present the high byte t_{RD1} from the falling edge of the $\overline{RD}$ pulse. $\overline{RD}$ is then applied for t_{VR} to complete reading of the current location.

Figure 20. Read Mode of Instruction ROM

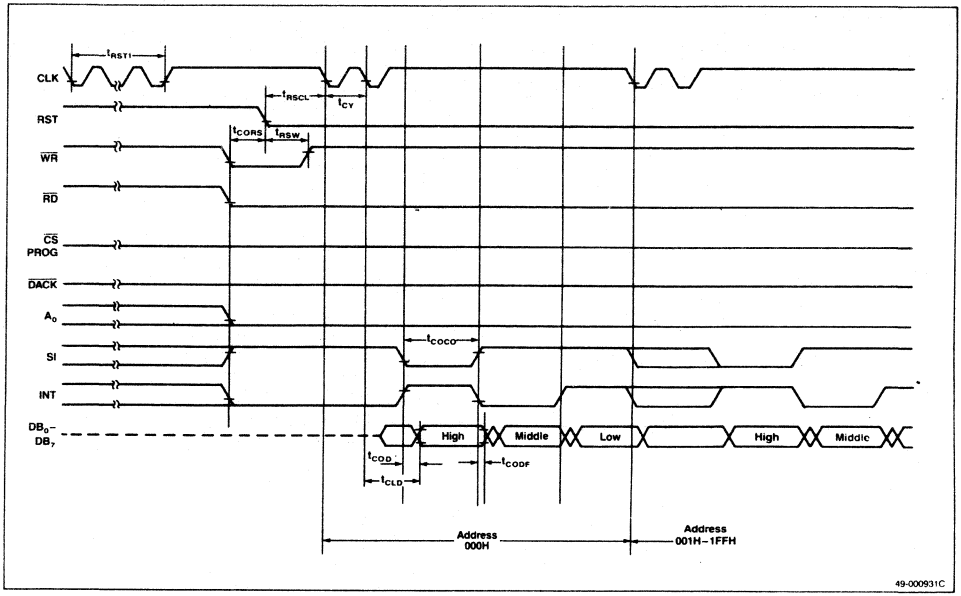
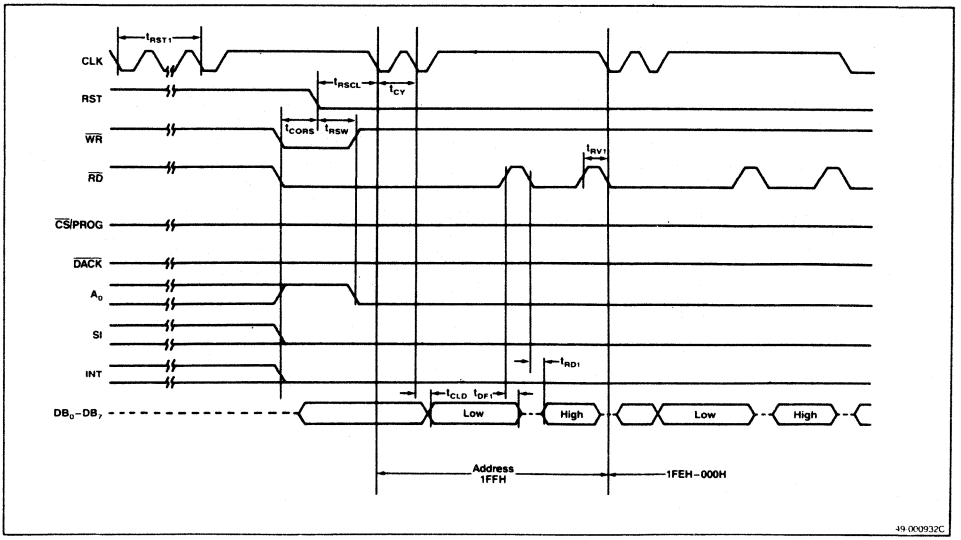


Figure 21. Read Mode of Data ROM



μPD77P20
Programming Operation, AC Characteristics

T_A = 25°C +5°C, V_{CC} = 5 V ± 5%, V_{PP} = 21 V ±0.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK cycle time	t_{CY}	240			ns	
CLK setup time to $\overline{RD}\downarrow$	t_{CLR}	2			μs	
CLK hold time From RST↓	t_{RSCL}	6			μs	
CLK hold time from PROG↓	t_{PRCL}	200			ns	
Control signal set-up time to RST↓	t_{CORS}	1			μs	
$\overline{WR}$ hold time from RST↓	t_{RSW}	6			μs	
Data set-up time from $\overline{RD}\downarrow$	t_{DRIO}	1			μs	
Data hold time from $\overline{RD}\downarrow$	t_{RD}	100			ns	
$\overline{RD}$ pulse width	t_{RR1}	1			μs	
SI, INT set-up time from $\overline{RD}\uparrow$	t_{COR}	100			ns	
SI, INT hold time from $\overline{RD}\downarrow$	t_{RCO}	100			ns	
$\overline{RD}$ set-up time To PROG↑	t_{RPR}	100			ns	
$\overline{RD}$ hold time from PROG↓	t_{PRR}	2			μs	
V_{PP} set-up time To PROG↑	t_{VPR}	2			μs	
V_{PP} hold time from PROG↓	t_{PRV}	2			μs	
RST pulse width	t_{RST1}	4			t_{CY}	
RST setup time	t_{RS}	1			μs	
PROG pulse width	t_{PRPR}	45	50	55	ms	

Read Operation, AC Characteristics

T_A = 25°C +5°C; V_{CC} = 5 V ±5%; V_{PP} = V_{CC} + 0.25 V max
V_{PP} = V_{CC} − 0.85 V min

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data access time from CLK	t_{CLD}			1	μs	
Data delay time from SI, IN↑	t_{COD}			1	μs	
Data float time from SI, IN↑	t_{CODF}	0			ns	
SI, INT pulse width	t_{COCO}	1			μs	
$\overline{RD}$ recovery time	t_{RV1}	500			ns	

Read Operation, AC Characteristics (cont)

T_A = 25°C +5°C; V_{CC} = 5 V ±5%; V_{PP} = V_{CC} + 0.25 V max
V_{PP} = V_{CC} − 0.85 V min

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data access time From $\overline{RD}\downarrow$	t_{RD1}			150	ns	
Data float time from $\overline{RD}\uparrow$	t_{DF1}	10			ns	

Operation Mode

The μPD77P20 may be utilized in an operation mode after the instruction ROM and data ROM have been programmed. Since it was first introduced in 1982, the μPD77P20 has undergone several mask revisions to improve manufacturability and/or function. And since the purpose of the μPD77P20 is to run any program that may be programmed in the masked ROM μPD7720A, it is important to know how to determine the step level, and the differences between them.

Date Code

The markings on the μPD77P20 package consist of three lines, as follows:

NEC JAPAN ← Manufacturer
D77P20D ← Part number
nnnnXnnnn ← Date code

The letter in the middle (e.g. 'X') of the date code identifies the step level of the part. Parts marked with step level K, E, or P should not be used for final system test by customers who are planning to submit code for the masked ROM μPD7720A.

On all other μPD77P20 stepping versions, a slight functional change was made, and the change is incorporated in the μPD7720A. The change allows the serial clock (SCK) to run asynchronously with CLK. Specified versions of μPD77P20 (i.e. K, E, P) and all Evakit-7720s and Evakit-7720Bs (Evaluation Systems for μPD7720A/μPD77P20) require that SCK run synchronously with CLK.

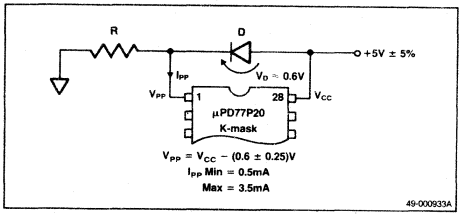
Because this functional change results in a slight change in internal serial timing, it is mandatory that code to be submitted for μPD7720A be verified in customer's system using versions of μPD77P20 other than those listed above (i.e. K, E, & P).

Pin 1 Connection

The K mask version requires that the programming voltage V_{PP} be supplied in a different manner than for all later versions, as shown in Figure 22. A silicon junction diode of 0.6 V forward voltage (V_F) should be used. R should be 800 to 1.8K Ω to satisfy the V_{PP} and I_{PP} requirements.

In all mask versions other than K, pin 1 must be connected directly to V_{CC}.

Figure 22. V_{PP} Circuitry for K Mask Version



μPD7720A and μPD77P20 Development Tools

For software development, assembly into object code, and debugging, an absolute assembler and simulator are available. The ASM77 Absolute Assembler and SIM77 Simulator for analyzing development code and I/O timing characteristics are available for systems supporting CP/M® and CP/M-86® (1), ISIS-II® (2), or MS-DOS® (3) operating systems. Additionally, the ASM77 Absolute Assembler is offered in Fortran source code for mini and main frame computer systems.

Once software development is complete, the code can be completely evaluated and debugged in hardware with the Evakit-7720 Evaluation System. The Evakit provides true in-circuit real-time emulation of the SPI for debugging and demonstrating your final system design. Code may be down-loaded to the Evakit from a development system via an RS232 port using the EVA communications program. This program is available in executable form for ISIS-II systems and many CP/M, CP/M-86, and MS-DOS systems. The EVA communications source code is also available for adapting the program to other systems.

The Evakit also serves to program the μPD77P20, a full-speed EPROM version of the SPI. A demonstration mask ROM chip, containing some common digital filtering routines, including N-stage IIR (biquadratic) and FIR (transversal filters), is available to test hardware interfaces to the SPI.

Further operational details of the SPI can be found in the μPD7720A Signal Processing Interface Technical Manual. Operation of the SPI development tools is described in the Absolute Assembler User Manual, the Simulator Operating Manual, and the Evakit-7720 User's Manual.

Note:

(1) CP/M and CP/M-86 are registered trademarks of Digital Research Corp.

(2) ISIS-II is a registered trademark of Intel Corp.

(3) MS-DOS is a registered trademark of Microsoft Corp.

System Configuration

Figures 23, 24, 25 and 26 show typical system applications for the μPD7720A and μPD77P20.

Figure 23. Spectrum Analysis System

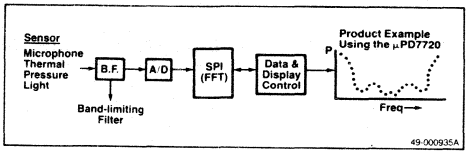


Figure 24. An Analog-to-Analog Digital Processing System Using a Single SPI

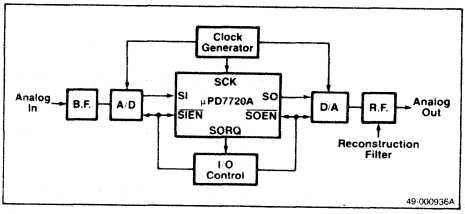


Figure 25. A Signal Processing System Using Cascaded SPIs & Serial Communication

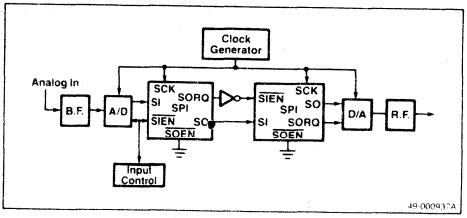
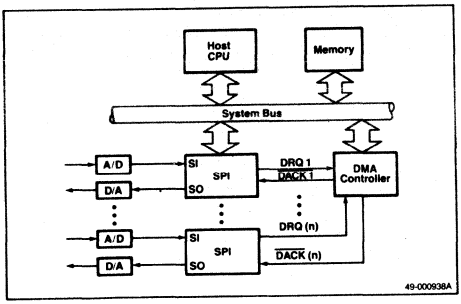
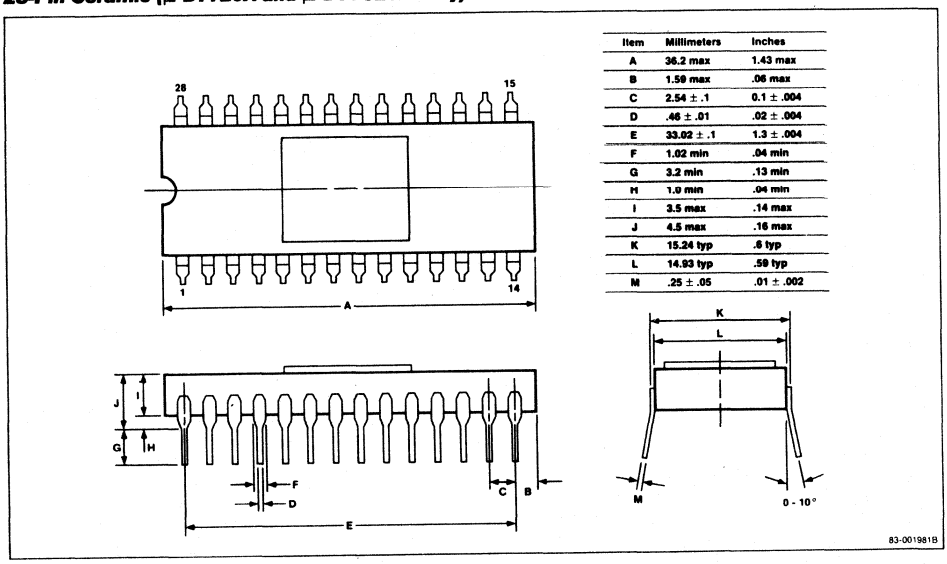


Figure 26. A Signal Processing System Using SPIs as a Complex Computer Peripheral



Packaging Information

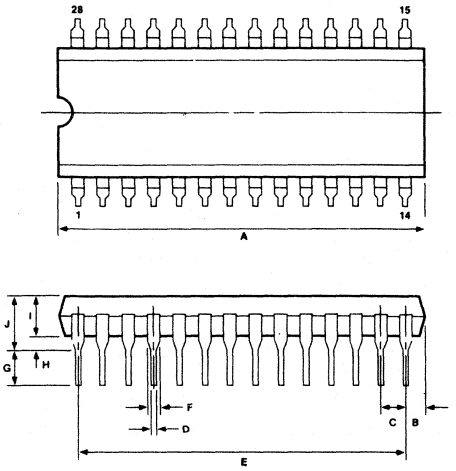
28-Pin Ceramic (μPD7720A and μPD77C20A Only)



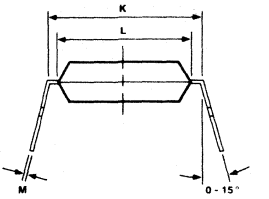
Item	Millimeters	Inches
A	36.2 max	1.43 max
B	1.58 max	.06 max
C	2.54 ± .1	0.1 ± .004
D	.46 ± .01	.02 ± .004
E	33.02 ± .1	1.3 ± .004
F	1.02 min	.04 min
G	3.2 min	.13 min
H	1.0 min	.04 min
I	3.5 max	.14 max
J	4.5 max	.16 max
K	15.24 typ	.6 typ
L	14.93 typ	.59 typ
M	.25 ± .05	.01 ± .002

Packaging Information (cont)

28-Pin Plastic (μPD7720A and μPD77C20A Only)



Item	Millimeters	Inches
A	38.1 max	1.5 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	33.02	1.3
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.72 max	.226 max
K	15.24 [TP]	.60 [TP]
L	13.2	.52
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$



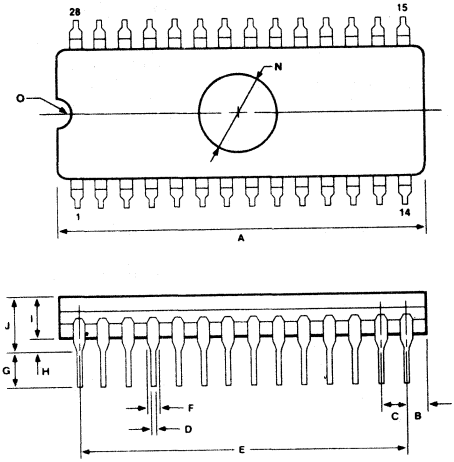
Notes: 1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

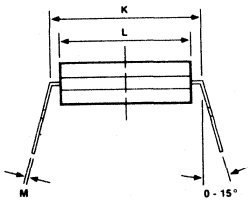
83-001407B

Packaging Information (cont)

28-Pin Cerdip (μPD77P20 Only)

Item	Millimeters	Inches
A	38.01 max	1.5 max
B	2.5	1
C	2.54 [T.P.]	.1 [T.P.]
D	.5 ± .1	.02 $^{+.004}_{-.005}$
E	33.02	1.3
F	1.3	.051
G	2.54 min	.1 min
H	.51 min	.02 min
I	4.57	.18
J	5.08 min	.2 min
K	15.24 [T.P.]	.6 [T.P.]
L	13.21 ± .5	.52 ± .02
M	.25 ± .05	.01 $^{+.002}_{-.003}$
N	7.62	.3
O	.65 rad	.026 rad



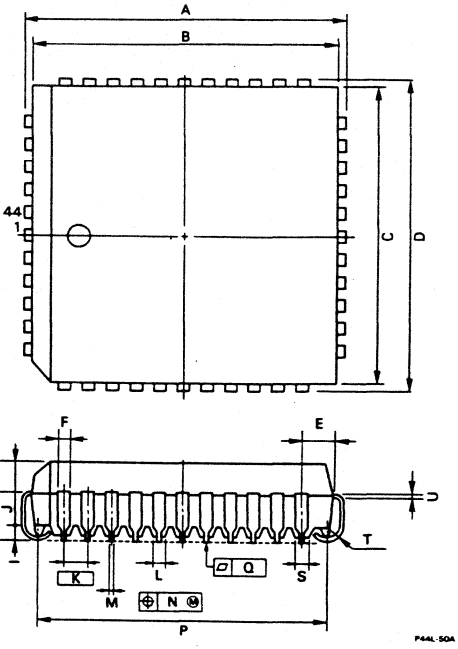


Note:

1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

83-003569B

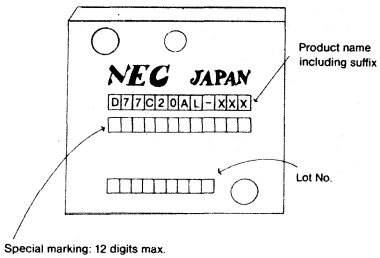
44-Pin PLCC (μPD7720AL and μPD77C20AL Only)



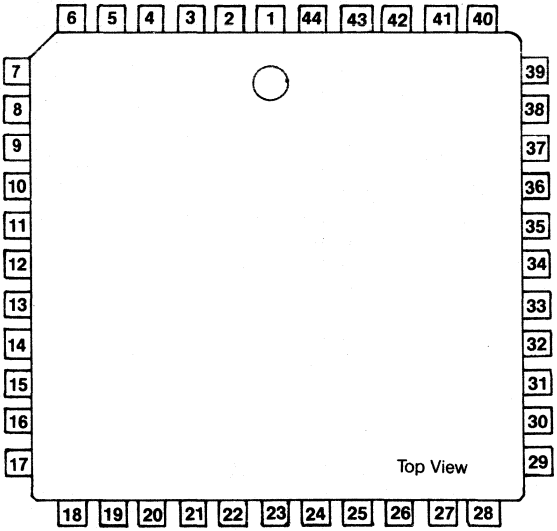
P44L-50A

NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.5±0.2	0.689±0.008
B	16.58	0.653
C	16.58	0.653
D	17.5±0.2	0.689±0.008
E	1.94±0.16	0.076±0.006
F	0.6	0.024
G	4.4±0.2	0.173±0.008
H	2.8±0.2	0.110±0.008
I	0.7 MIN	0.028 MIN
J	3.6	0.142
K	1.27 (T.P.)	0.050 (T.P.)
L	0.7	0.028
M	0.40±0.10	0.016±0.004
N	0.12	0.005
P	15.50±0.30	0.610±0.012
Q	0.15	0.006
S	1.0	0.040
T	R 0.8	R 0.031
U	0.20±0.10	0.008±0.004



44-Pin PLCC (μPD7720AL and μPD77C20AL Only)



PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	VCC	12	D2	23	NC	34	NC
2	NC	13	D3	24	CLK	35	SO
3	DACK	14	D4	25	RST	36	SORC
4	DRQ	15	NC	26	NC	37	WR
5	PO	16	D5	27	INT	38	RD
6	NC	17	NC	28	SCK	39	NC
7	NC	18	NC	29	NC	40	NC
8	P1	19	D6	30	SIEN	41	CS
9	D0	20	D7	31	SOEN	42	AO
10	NC	21	GND	32	NC	43	NC
11	D1	22	GND	33	SI	44	VCC

μPD77C20A

Absolute Maximum Ratings*

T_a = 25°C	
Voltage (V_{CC} Pin)	−0.5 to +7.0V ①
Voltage, Any Input	−0,5 to V_{CC} + 0,3
Voltage, Any Output	−0.5 to V_{CC} + 0,3
Operating Temperature	−40°C to + 85°C
Storage Temperature	−65°C to +150°C

Note: ① With respect to GND.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

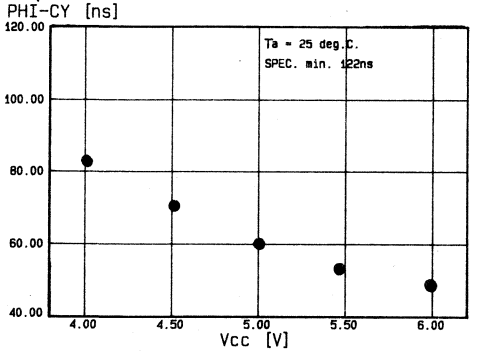
T_a = −40°C to +85°C, V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} +0.5	V	
CLK Low Voltage	$V\phi_L$	−0.5		0.45	V	
CLK High Voltage	$V\phi_H$	3.5		V_{CC} +0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{LIL}			−10	μA	V_{IN} = 0V
Input Load Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Output Float Leakage	I_{LOL}			−10	μA	V_{OUT} = 0.47V
Output Float Leakage	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Power Supply Current	I_{CC}		120	170	mA	

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK, SCK Input Capacitance	$C\phi$			20	pF	T_a = 25°C
Input Pin Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Output Pin Capacitance	C_{OUT}			20	pF	V_{CC} = 0V

μPD77C20A CLOCK vs. SUPPLY VOLTAGE

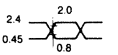


AC Characteristics

T_a = −40°C to +85°C, V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK Cycle Time	ϕCY	120		2000	ns	①
CLK Pulse Width	ϕD	50			ns	
CLK Rise Time	ϕR			10	ns	①
CLK Fall Time	ϕF			10	ns	①
Address Setup Time for $\overline{RD}$	t_{AR}	0			ns	
Address Hold Time for $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{RD}$	t_{RD}			150	ns	C_L = 100 pF
Read to Data Floating	t_{DF}	10		100	ns	C_L = 100 pF
Address Setup Time for $\overline{WR}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	250			ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0			ns	
$\overline{RD}$, $\overline{WR}$, Recovery Time	t_{RV}	250			ns	②
DRQ Delay	t_{AM}			150	ns	C_L = 100 pF
$\overline{DACK}$ Delay Time	t_{DACK}	1			ϕD	②
$\overline{DACK}$ Pulse Width	t_{DD}	250		∞	ns	③
SCK Cycle Time	t_{SCY}	480		DC	ns	
SCK Pulse Width	t_{SCK}	230			ns	
SCK Rise/Fall Time	t_{RSC}			20	ns	①
SORQ Delay ↑	t_{DRQ}	30		150	ns	C_L = 100 pF
$\overline{SOEN}$ Setup Time	t_{SOC}	50			ns	
$\overline{SOEN}$ Hold Time	t_{CSO}	30			ns	
SO Delay from SCK = LOW	t_{DCK}			150	ns	
SO Delay from SCK with SORQ ↑	t_{DZRQ}	20		300	ns	②
SO Delay from SCK	t_{DZSC}	20		300	ns	②
SO Delay from $\overline{SOEN}$	t_{DZE}	20		180	ns	②
$\overline{SOEN}$ to SO Floating	t_{HZE}	20		200	ns	②
SCK to SO Floating	t_{HZSC}	20		300	ns	②
SO Delay from SCK with SORQ ↓	t_{HZRQ}	70		300	ns	②
$\overline{SIEN}$, SI Setup Time	t_{DC}	55			ns	②
$\overline{SIEN}$, SI Hold Time	t_{CD}	30			ns	
P_0, P_1 Delay	t_{DP}			ϕCY + 150	ns	
RST Pulse Width	t_{RST}	4			ϕCY	
INT Pulse Width	t_{INT}	8			ϕCY	

Notes: ① Voltage at measuring point of timing 1.0V and 3.0V
② Voltage at measuring point of AC Timing
V_{IL} = V_{OL} = 0.8V
V_{IH} = V_{OH} = 2.0V
Input Waveform of AC Test (except CLK, SCK)



③ In 16 bit DMA mode only

Note: μPD7720AD, low-power NMOS version in ceramic package, functions at full speed 8 MHz over the −45° to +85° C temperature range.

7720AD Extended Temperature Specification

Absolute Maximum Ratings

Voltage, V_{CC} Pin	−0.5 to +7.0V	*1
Voltage, Any Input	−0.5 to +7.0V	*1
Voltage, Any Output	−0.5 to +7.0V	*1
Operating Temperature	−10 to +70°C	
– Extended Temperature	−40 to +85°C	
– Very Extended Temperature	−40 to +110°C	*2
– Super Extended Temperature	−55 to +125°C	*2
Storage Temperature	−65°C to +150°C	

*1 With respect to GND at +25°C

*2 Any devices are not tested at these temperature

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK, SCK Input Capacitance	C_{ϕ}			20	pF	
Input Pin Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Output Pin Capacitance	C_{OUT}			20	pF	

DC Characteristics

V_{CC} = 5.0V ± 5%

Parameter	Symbol	Temperature Limits STD −10/+70 Min	Max	EXT −40/+85 Min	Max	VEXT −40/+110 Min	Max	SEXT −55/+125 Min	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}		0.8		0.8		0.6		0.6	V	
Input High Voltage	V_{IH}	2.0		2.0		2.2		2.2		V	
CLK Low Voltage	$V_{\phi L}$		0.45		0.45		0.4		0.4	V	
CLK High Voltage	$V_{\phi H}$	3.5		3.5		3.7		3.7		V	
Output Low Voltage	V_{OL}		0.45		0.45		0.5		0.5	V	I_{OL} = 2.0mA
Output High Voltage	V_{OH}	2.4		2.4		2.3		2.3		V	I_{OH} = −400 μA
Input Load Current	I_{LIL}		−10		−10		−10		−10	μA	V_{IN} = 0V
Input Load Current	I_{LIH}		10		10		10		10	μA	V_{IN} = V_{CC}
Output Float Leakage	I_{LOL}		−10		−10		−10		−10	μA	V_{OUT} = 0.47V
Output Float Leakage	I_{LOH}		10		10		10		10	μA	V_{OUT} = V_{CC}
Power Supply Current	I_{CC}		170		200		200		200	mA	

μPD7720AD Extended Temperature Specification

AC Characteristics

$V_{CC} = 5.0V \pm 5\%$

Parameter	Symbol	Temperature Limits: STD −10/+70 and EXT −40/+85 Min	STD −10/+70 and EXT −40/+85 Max	VEXT −40/+110 Min	VEXT −40/+110 Max	SEXT −55/+125 Min	SEXT −55/+125 Max	Unit	Test Conditions
CLK Cycle Time	ϕ CY	122	2000	152	1000	162	1000	ns	*3
CLK Pulse Width	ϕ D	60		75		80		ns	
CLK Rise Time	ϕ R		10		10		10	ns	*3
CLK Fall Time	ϕ F		10		10		10	ns	*3
Address Setup Time for $\overline{RD}$	t_{AR}	0		50		50		ns	
Address Hold Time for $\overline{RD}$	t_{RA}	0		0		0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		300		320		ns	
Data Delay from $\overline{RD}$	t_{RD}		150		170		180	ns	$C_L = 100$ pF
Read to Data Floating	t_{DF}	10	100	10	120	10	130	ns	$C_L = 100$ pF
Address Setup Time for $\overline{WR}$	t_{AW}	0		50		50		ns	
Address Hold Time for $\overline{WR}$	t_{WA}	0		0		0		ns	
$\overline{WR}$ Pulse Width	t_{WW}	250		300		320		ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150		170		180		ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0		50		50		ns	
$\overline{RD}$, $\overline{WR}$, Recovery Time	t_{RV}	250		300		320		ns	*4
DRQ Delay	t_{AM}		150		170		180	ns	
$\overline{DACK}$ Delay Time	t_{DACK}	1		1		1		D	*4
SCK Cycle Time	t_{SCY}	480	DC	600	DC	640	DC	ns	
SCK Rise/fall Time	t_{RSC}		20		20		20	ns	*3
SORQ Delay	t_{DRQ}	30	150	10	170	10	180	ns	$C_L = 100$ pF
$\overline{SOEN}$ Setup Time	t_{SOC}	50		80		100		ns	
$\overline{SOEN}$ Hold Time	t_{CSO}	30		50		60		ns	
SO Delay from SCK = LOW	t_{DCK}		150		170		180	ns	
SO Delay from SCK with SORQ	t_{DZRQ}	20	300	10	350	10	350	ns	*4
SO Delay from SCK	t_{DZSC}	20	300	10	350	10	350	ns	*4
SO Delay from $\overline{SOEN}$	t_{DZE}	20	180	10	230	10	230	ns	*4
$\overline{SOEN}$ to SO Floating	t_{HZE}	20	200	10	250	10	250	ns	*4
SCK to SO Floating	t_{HZSC}	20	300	10	350	10	350	ns	*4
SO Delay from SCK with SORQ	t_{HZRQ}	70	300	60	350	60	350	ns	*4
$\overline{SIEN}$, SI Setup Time	t_{DC}	55		85		105		ns	
$\overline{SIEN}$, SI Hold Time	t_{CD}	30		50		60		ns	
P_0, P_1 Delay	t_{DP}		ϕCD +150		ϕCD +170		ϕCD +180	ns	
RST Pulse Width	t_{RST}	4		4		4		ϕCY	
INT Pulse Width	t_{INT}	8		8		8		ϕCY	
SCK Pulse Width	t_{SCK}	230		290		310		ns	
$\overline{DACK}$ Pulse Width	t_{DD}	250	2000	280	20000	280	2000	ns	

*3 Voltage at measuring point of timing 1.0 V and 3.0 V
*4 Voltage at measuring point of AC Timing
$V_{IL} = V_{OL} = 0.8V$
$V_{IH} = V_{CH} = 2.0V$

Input Waveform of AC Test (except CLK, SCK)

μPD7720AC Extended Temperature Specification

Absolute Maximum Ratings

Voltage (V_{CC} Pin)	−0.5 to +7.0V *
Voltage, Any Input	−0.5 to +7.0V *
Voltage, Any Output	−0.5 to +7.0V *
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°

* With respect to GND

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK, SCK Input Capacitance	C_ϕ			20	pF	
Input Pin Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Output Pin Capacitance	C_{OUT}			20	pF	

DC Characteristics

V_{CC} = +5.0V ± 5%

Parameter	Symbol	Limits STD −10/+70 Min	Max	(M) −40/+85 Min	Max	Unit	Test Conditions
Input Load Current	V_{IL}		0.8		0.8	V	
Input Load Current	V_{IH}	2.0		2.0		V	
Output Float Leakage	$V_{\phi L}$		0.45		0.45	V	
Output Float Leakage	$V_{\phi H}$	3.5		3.5		V	
Power Supply Current	V_{OL}		0.45		0.45	V	I_{OL} = 2.0mA
Input Low Voltage	V_{OH}	2.4		2.4		V	I_{OH} = 400μA
Input High Voltage	I_{LIL}		−10		−10	μA	V_{IN} = 0V
CLK Low Voltage	I_{LIH}		10		10	μA	V_{IN} = V_{CC}
CLK High Voltage	I_{LOL}		−10		−10	μA	V_{OUT} = 0.47V
Output Low Voltage	I_{LOH}		10		10	μA	V_{OUT} = V_{CC}
Output High Voltage	I_{CC}		170		200	mA	

AC Characteristics

V_{CC} = +5.0V ± 5%

Parameter	Symbol	Limits STD −10/+70 Min	Max	(M) −40/+85 Min	Max	Unit	Test Conditions
CLK Cycle Time	ϕCY	122	2000	140	2000	ns	*3
CLK Pulse Width	ϕD	60		70		ns	
CLK Rise Time	ϕR		10		10	ns	*3
CLK Fall Time	ϕF		10		10	ns	*3
Address Setup Time for $\overline{RD}$	t_{AR}	0		0		ns	
Address Hold Time for $\overline{RD}$	t_{RA}	0		0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		280		ns	
Data Delay from $\overline{RD}$	t_{RD}		150		160	ns	C_L = 100 pF
Read to Data Floating	t_{DF}	10	100	10	110	ns	C_L = 100 pF
Address Setup Time for $\overline{WR}$	t_{AW}	0		0		ns	
Adress Hold Time for $\overline{WR}$	t_{WA}	0		0		ns	
$\overline{WR}$ Pulse Width	t_{WW}	250		280		ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150		160		ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0		0		ns	
$\overline{RD}$, $\overline{WR}$, Recovery Time	t_{RV}	250		280		ns	*4
DRQ Delay	t_{AM}		150		160	ns	
$\overline{DACK}$ Delay Time	t_{DACK}	1		1		ϕD	*4
SCK Cycle Time	t_{SCY}	480	DC 560		DC	ns	
SCK Rise/Fall Time	t_{RSC}		20		20	ns	*3
SORQ Delay	t_{DRQ}	30	150	20	160	ns	C_L = 100 pF
$\overline{SOEN}$ Setup Time	t_{SOC}	50		60		ns	
$\overline{SOEN}$ Hold Time	t_{CSO}	30		40		ns	
SO Delay from SCK = LOW	t_{DCK}		150		160	ns	
SO Delay from SCK with SORQ	t_{DZRQ}	20	300	20	300	ns	*4
SO Delay from SCK	t_{DZSC}	20	300	20	300	ns	*4
SO Delay from $\overline{SOEN}$	t_{DZE}	20	180	20	180	ns	*4
$\overline{SOEN}$ to SO Floating	t_{HZE}	20	200	20	200	ns	*4
SCK to SO Floating	t_{HZSC}	20	300	20	300	ns	*4
SO Delay from SCK with SORQ	t_{HZRQ}	70	300	60	300	ns	*4
$\overline{SIEN}$, SI Setup Time	t_{DC}	55		75		ns	
$\overline{SIEN}$, SI Hold Time	t_{CD}	30		40		ns	
P_0, P_1 Delay	t_{DP}		ϕCD +150		ϕCD +150	ns	
RST Pulse Width	t_{RST}	4		4		ϕCY	
INT Pulse Width	t_{INT}	8		8		ϕCY	
SCK Pulse Width	t_{SCK}	230		270		ns	
$\overline{DACK}$ Pulse Width	t_{DD}	250	2000	280	2000	ns	

Description

The μPD77230 Advanced Signal Processor (ASP) is the high-end member of a new third-generation family of 32-bit digital signal processors. This CMOS chip implements 32-bit full floating-point arithmetic, and is intended for digital signal processing and other applications requiring high speed and high precision.

All instructions execute in one instruction cycle. The μPD77230 executes a 32-bit by 32-bit floating point multiply with 55-bit product, sum of products, data move, and multiple data pointer manipulations—all in one 150-ns instruction cycle.

Features

- ☐ Fast instruction cycle: 150 ns using 13.3-MHz clock
- ☐ All instructions execute in one cycle
- ☐ 32- x 32-bit floating point arithmetic
- ☐ Large on-chip memory (32-bit words)
  - — 1K data RAM (two 512-word blocks)
  - — 1K data coefficient ROM
  - — 2K instruction ROM
- ☐ 8K- x 32-bit external memory; 4K may be instruction memory
- ☐ 1.5-μm CMOS technology
- ☐ 32-bit internal bus
- ☐ 55-bit ALU bus
- ☐ Dedicated internal buses for RAM, multiplier, and ALU
- ☐ Eight accumulators/working registers (55 bits)
- ☐ 47-bit bidirectional barrel shifter
- ☐ Two independent data RAM pointers
- ☐ Modulo 2^n incrementing for circular RAM buffers
- ☐ Base and index addressing of internal RAM
- ☐ Data ROM capable of 2^n incrementing
- ☐ Loop counter for repetitive processing
- ☐ Eight-level stack accessible to internal bus
- ☐ Two interrupts: maskable and nonmaskable (NMI)
- ☐ Serial I/O (5 MHz)
- ☐ Master/slave mode operation
- ☐ Three-stage instruction pipeline
- ☐ Single +5-volt power supply
- ☐ Approximately 1.2 watts

Ordering Information

Part Number	Package Type
μPD77230R	68-pin PGA

Applications

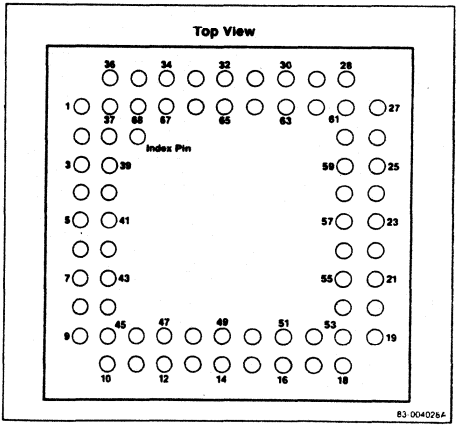
- ☐ General-purpose digital filtering (FIR, IIR, FFT)
- ☐ High-speed data modems
- ☐ Adaptive equalization (CCITT)
- ☐ Echo cancelling
- ☐ High-speed controls
- ☐ Image processing
- ☐ Graphic transformations
- ☐ Instrumentation electronics
- ☐ Numerical processing
- ☐ Speech processing
- ☐ Sonar/radar signal processing
- ☐ Waveform generation

Floating-Point Performance Benchmarks

Second-order digital filter (biquad)	0.9 μs
32-tap finite impulse response filter	5.25 μs
Fast Fourier transform (FFT)	
32-point complex (radix 2)	0.15 ms
512-point complex FFT	4.7 ms
1024-point complex FFT	10.75 ms
Square root	6.0 μs

Pin Configuration

68-Pin PGA



Pin Identification

No.	Master	*Slave	No.	Master	*Slave
1	D_0		35	D_2	
2	A_1		36	D_1	
3	A_3		37	A_0	
4	A_5		38	A_2	
5	A_6		39	A_4	
6	A_8		40	V_{DD}	
7	A_{10}		41	A_7	
8	A_X		42	A_9	
9	WR		43	A_{11}	
10	RD		44	GND	
11	SORQ		45	SO	
12	SOCK		46	SICK	
13	SOEN		47	SIEN	
14	INT		48	NC (No connection)	
15	INTM		49	RESET	
16	M/S		50	SI	
17	CLKOUT		51	X2	
18	X1		52	V_{DD}	
19	D_{31}	P3	53	D_{30}	P2
20	D_{29}	P1	54	D_{28}	P0
21	D_{27}	RQM	55	D_{26}	CS
22	D_{25}	HWR	56	GND	
23	D_{24}	HRD	57	D_{23}	I/O_{15}
24	D_{22}	I/O_{14}	58	D_{21}	I/O_{13}
25	D_{20}	I/O_{12}	59	D_{19}	I/O_{11}
26	D_{18}	I/O_{10}	60	V_{DD}	
27	D_{17}	I/O_9	61	D_{15}	I/O_7
28	D_{16}	I/O_8	62	D_{13}	I/O_5
29	D_{14}	I/O_6	63	D_{11}	I/O_3
30	D_{12}	I/O_4	64	D_9	I/O_1
31	D_{10}	I/O_2	65	D_7	
32	D_8	I/O_0	66	D_5	
33	D_6		67	D_3	
34	D_4		68	GND	

*If slave-mode pin identification is not specified, it is the same as master-mode.

Pin Function Summary

Symbol	I/O	Function
A_0-A_{11}	O	Address bus to external memory
A_X	O	Highest bit of memory address
CLKOUT	O	Internal system clock
CS	I	Chip select
D_0-D_7	I/O*	Data bus for access to external memory in slave mode.
D_0-D_{31}	I/O*	Data bus for access to external memory (data or instruction) in master mode.
GND		Ground (Connect ground to all GND pins.)
HRD	I	Host CPU read
HWR	I	Host CPU write
I/O_0-I/O_{15}	I/O*	Port to host CPU data bus
INT	I	Nonmaskable interrupt
INTM	I	Maskable interrupt
M/S	I	Operation mode select
P0, P1	I	General-purpose input port
P2, P3	O	General-purpose output port
RD	O	Controls data read from external memory
RESET	I	System reset
RQM	O	Data read/write request
SI	I	Serial input data
SICK	I/O	Clock for serial input data
SIEN	I	Serial input data enable
SO	O*	Serial output data
SOCK	I/O	Clock for serial output data
SOEN	I	Serial output data enable
SORQ	O	Serial output request
V_{DD}		+5-volt power (Connect +5 V to all V_{DD} pins.)
WR	O	Controls data write to external memory
X1, X2	I	External clock (X1) or crystal (X1, X2)

*These pins have a high-impedance inactive state.

Pin Functions

Paragraphs below supplement the brief descriptions in the preceding table. Pin symbols are in alphabetical order within several master and slave mode categories.

Master and Slave Modes

CLKOUT [System Clock]. Outputs internal system clock. Output signal frequency is half the oscillation frequency of crystal connected across X1 and X2 pins.

INT [Nonmaskable Interrupt]. Inputs nonmaskable interrupt signal, which is active-low and must be at least three system clock pulses wide. Interrupt signal is detected at falling edge. Interrupt address is 10H.

INTM [Maskable Interrupt]. Inputs maskable interrupt signal, which is active-low and must be at least three system clock pulses wide. Interrupt signal is detected at falling edge. Interrupt address is 100H.

M/S [Mode Select]. Selects operation mode. Operation mode must not be switched during operation, however. Master = 0; slave = 1.

RESET [System Reset]. Inputs internal system reset signal, which is active-low and must be at least three system clock pulses wide.

SI [Serial Input Data]. Inputs serial data synchronized with falling edge of SICK.

SICK [Serial Input Clock]. Inputs or outputs clock for serial input data. Serial data is internally latched at the falling edge of the clock that is input to or output from this pin. Whether the clock is to be input from an external source or the internal clock is to be output is determined by the status register setting.

SIEN [Serial Input Enable]. Enables SI pin to input serial data. This pin is active-low.

SO [Serial Output Data]. Outputs serial data synchronized with rising edge of SOCK pin.

SOCK [Serial Output Clock]. Inputs or outputs clock for serial output data. The serial output data is synchronized with the clock that is input to or output from this pin. Whether the clock is to be input from an external source or the internal clock is to be output is determined by the status register setting.

SOEN [Serial Output Enable]. Enables SO pin to output serial data. This pin is active-low.

SORQ [Serial Output Request]. Outputs serial output request signal, which is active-high. When data is ready in the serial output register, this signal becomes 1. It will become 0 after data has been output.

X1, X2 [External Clock]. Connection to external oscillator crystal (X1, X2) or external clock (X1).

Master Mode, External Memory Interface

A_0-A_{11} [Address Bus]. Address bus for access to external memory. When accessing external instruction memory, the lower 12 bits of the program counter are output to these pins. When accessing external data memory, the lower 12 bits of the external address register are output to these pins.

A_X [Highest Address Bit]. Outputs the highest bit of the memory address. When accessing external instruction memory, the highest bit of the program counter (PC_{12}) is output to this pin. When accessing external data memory, the highest bit of the external address register is output to this pin. High-speed memory area = 0; low-speed memory area = 1.

D_0-D_{31} [Data Bus]. These pins form a 32-bit data bus for external memory (data or instruction).

RD [Data Read]. Controls data read from external memory. This signal becomes 0 after the output address is valid, and data is input at the rising edge to the data port formed by pins D_0 to D_{31}.

WR [Data Write]. Controls data write to external memory. This signal becomes 0 after the output address is valid and data is output to the data port formed by pins D_0 to D_{31}.

Slave Mode, External Memory Interface

A_0-A_{11} [Address Bus]. Address bus for accessing external memory. When accessing external data memory, the lower 12 bits of the external address register are output to these pins.

A_X [Highest Address Bit]. When accessing external data memory, the highest bit of the external address register is output to this pin. High-speed memory area = 0; low-speed memory area = 1.

D_0-D_7 [Data Bus]. These pins form an eight-bit data bus for external data memory access. Data may be transferred in one of four formats (1-, 2-, 3-, or 4-byte words), depending on the status register setting.

RD [Data Read]. Controls data read from external memory. This signal becomes 0 after the output address is valid, and data is input at the rising edge to the data port formed by pins D_0 to D_7.

WR [Data Write]. Controls data write tc external memory. This signal becomes 0 after the output address is valid and data is output to the data port formed by pins D_0 to D_7.

Slave Mode, Host CPU Interface

CS [Chip Select]. Active-low chip select input signal. When this pin becomes 0, the host CPU may perform read/write operations on the 16-bit port formed by pins I/O_0 through I/O_{15}.

HRD [Host CPU Read]. Active-low host read input signal. In conjunction with CS, this signal allows the host CPU to read data from the DRS register via the 16-bit port formed by pins I/O_0 to I/O_{15}.

HWR [Host CPU Write]. Active-low host write input signal. In conjunction with CS, this signal allows the host CPU to write data into the DRS register via the 16-bit port formed by pins I/O_0 to I/O_{15}.

I/O_0-I/O_{15} [Data Port]. These pins form an I/O port to the host CPU bidirectional data bus. It is used for input to or output from the DRA register under control of host CPU signals CS, HWR, and HRD. Data transfer format can be specified in the status register as either a 16-bit or a 32-bit transfer.

RQM [Read/Write Request]. Requests host CPU to read or write data via the host CPU data bus.

Slave Mode, I/O Port

P0, P1 [Input Port]. These pins form a general-purpose input port. Status of either of these pins may be tested by a conditional branch instruction.

P2, P3 [Output Port]. These pins form a general-purpose output port. Data output by these pins can be set directly by an instruction and will be retained until explicitly changed.

Functional Description

Figure 1 is the functional block diagram of the μPD77230 in its master mode configuration. The main internal bus (32 bits) ties together all the functional blocks of the μPD77230, including the ALU area. The 55-bit processing unit (PU) bus links the ALU input to the 55-bit multiplier output register and the eight 55-bit working registers. Thus, the full 55 bits of precision can be maintained during extensive calculations.

In addition to the main bus and the PU bus, there is a sub-bus linking each of the two RAM areas to both the ALU input and the multiplier input registers. This allows simultaneous loading of the multiplier input registers in parallel with ALU operations and in parallel with data transfer operations, which make use of the main bus. There is a sub-bus connecting the ALU input to the 55-bit multiplier output and another sub-bus that can route the working registers' contents back to the ALU input.

Architecture

The μPD77230 has a Harvard-type architecture, with separate memory areas for program storage and data storage as well as separate, multiple buses. A multiple-stage instruction execution pipelining scheme performs instruction fetch and execution in parallel. All instructions are executed in a single cycle, even if the instruction is stored in the external instruction memory expansion area.

Instruction Memory

The μPD77230 has an internal instruction ROM that holds 2K 32-bit instruction words. An additional 4K word external memory expansion is also available. A 13-bit program counter (PC) contains the current instruction address; the most significant bit of the PC determines whether on-chip or external instructions are to be fetched. An eight-level stack holds subroutine and interrupt return addresses, and it is accessible to/from the main internal bus.

Data Memory

The data ROM area on the μPD77230 holds 1K 32-bit words. The ROM pointer (RP) contains the current ROM address, which can also be specified within an instruction field. The ROM pointer has auto-increment and auto-decrement features and an add 2^n to the RP option.

There are two separate and independently addressable data RAM areas, each 512 words by 32 bits. Each RAM area can be addressed by a base register, an index register, or the sum of the two. The base register and/or the index register may be incremented, decremented, or cleared. In addition, the base pointer can operate in a modulo count mode, and the index register contents may be replaced by the sum of the index and base registers.

Data memory may be expanded by the addition of 8K words of external memory. External data memory is divided into a high-speed half, which is accessed in a single instruction cycle, and a low-speed half, which is accessed in three instruction cycles. Both high-speed and low-speed memory accesses occur in parallel with normal program execution.

Multiplier and ALU

The floating-point multiplier has two 32-bit input registers, called the K and L registers, which are accessible both to and from the main bus. The multiplier produces the 55-bit product of the K and L register contents automatically in a single instruction cycle (there is no multiply instruction). The 55-bit result is

stored in the M register in 8-bit exponent, 47-bit mantissa format. The contents of the M register can be transferred to the main bus (32 bits) or to the ALU via the processing unit bus (55 bits). The multiplier consists of a 24- by 24-bit fixed-point multiplier and an exponent adder, so that it can also be used for fixed-point multiplications.

The 55-bit floating-point ALU is capable of a full set of arithmetic and logical operations (see Instruction Set section). There is a 47-bit bidirectional barrel shifter, which can perform general-purpose shifting in addition to the mantissa alignments required for floating-point arithmetic. A separate exponent ALU (EALU) determines shift values in floating-point work. The ALU status is reflected in one of two identical processor status words (PSW) that contain carry, zero, sign, and overflow flags. The results of the ALU operation are stored in one of eight 55-bit accumulators or "working registers."

There are two 55-bit input registers to the ALU called the P register and the Q register. The Q register input is selected from one of the eight working registers, while the P register input is selected from among the 32-bit main bus, data RAM 0, data RAM 1, and the 55-bit M register.

A loop counter is included in the design of the μPD77230. This loop counter is a 10-bit register, attached to the main bus, which can be decremented by a control bit built into an ordinary ALU instruction. When the loop counter is decremented to zero, the instruction following the one that decremented it will be skipped.

System Control

The master system clock may be provided to the μPD77230 via either an external crystal or an already available clock signal. The internal clock of the μPD77230 contains two phases, and is obtained by dividing the master clock frequency by 2. If desired, the serial input and output clocks can be derived from the master clock by dividing it by 8.

Both a maskable and nonmaskable interrupt are available in the μPD77230. The maskable interrupt can be "memorized," so that if an interrupt occurs while it is in the interrupt disabled condition, then it may be acted upon (or disregarded) at a later time. The status of the interrupts and other aspects of the μPD77230 are determined by or reflected in the 20-bit status register.

Serial I/O

The serial input and output circuitry in the μPD77230 is designed for easy interfacing to codecs and other μPD77230s. The input and output circuits are independently clocked by either an internal clock or an external clock up to 5 MHz. The length of the serial input and output data words can be independently programmed to be 8, 16, 24, or 32 bits.

The parallel I/O capabilities in the μPD77230 can be used for external instruction and data memory expansion and for interaction with a host processor. The difference between master mode and slave mode operation must be defined to further discuss the nature of the parallel interface in the μPD77230.

Master/Slave Modes

The master mode parallel interface is shown in figure 1. In this mode, the μPD77230 is intended to act as a standalone processor with the parallel interface allowing access to external memory, memory-mapped I/O devices, and/or a system-level bus. Master mode operation allows for external instruction memory expansion and external data memory expansion. There is an 8K external memory space. The lower 4K can be shared between instructions and data, while the upper 4K can be used for data only.

The slave mode parallel interface is shown in figure 2. In this mode, the μPD77230 is a "peripheral" to a host processor. The full 8K external memory space is available for data memory expansion, but instruction memory expansion is not allowed in slave mode. The 8-bit external data bus is used to assemble words in the data register (DR), which can be 8, 16, 24 or 32 bits wide. Communication with the host occurs across the 16-bit host data bus. Word lengths of 16 or 32 bits can be transferred between the μPD77230 and the host. Four pins can be used in slave mode as general-purpose I/O ports: two input pins and two output pins.

Figure 3 shows the functional pin groups in master mode and slave mode.

Figure 1. Master Mode Block Diagram

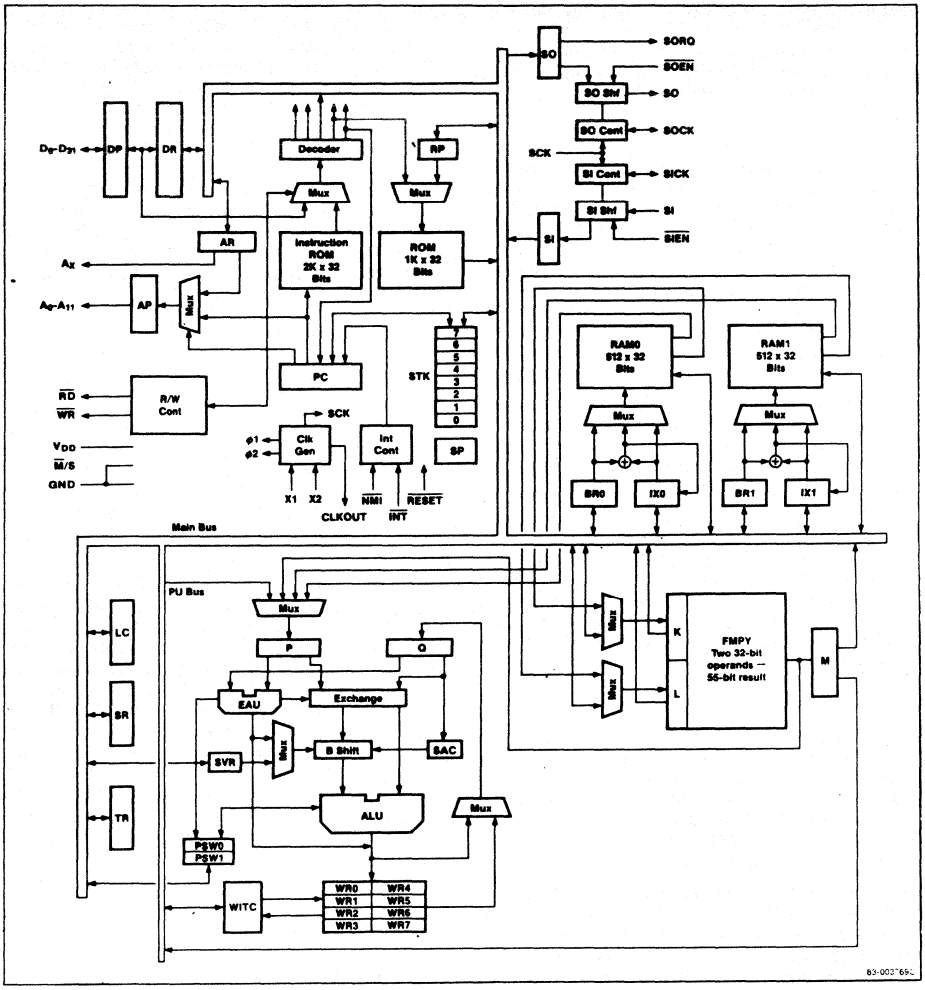


Figure 2. Slave Mode Block Diagram

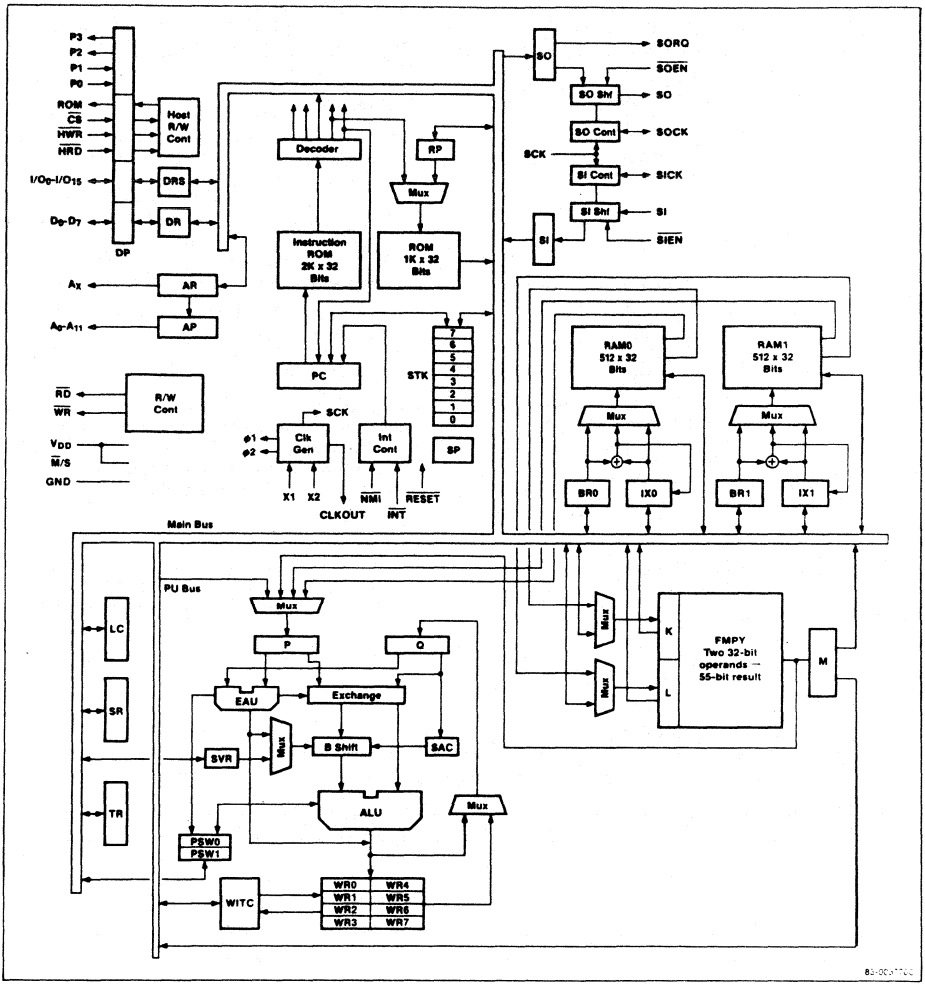
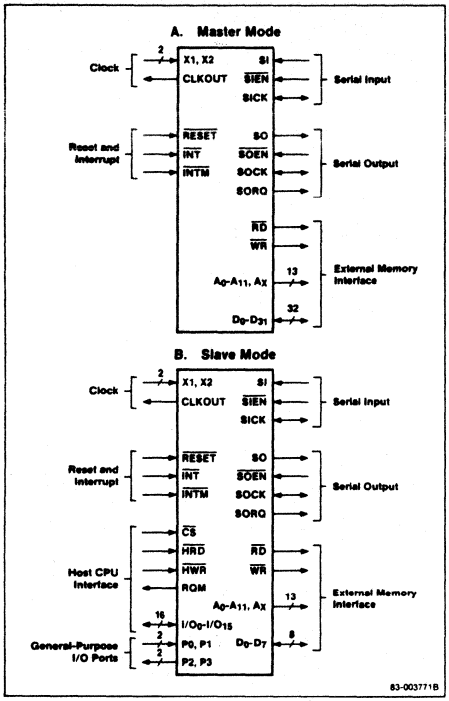


Figure 3. Functional Pin Groups



Instruction Set

All μPD77230 instructions consist of a single 32-bit word. Figure 4 shows the bit format for the three basic types of instructions.

OP Type Instruction

This is an ALU operation instruction where 26 different operations may be specified in the upper five bits (figure 4). Pointer modifications may be specified in the CNT field. Transfers may also be specified within an OP instruction by use of the SRC and DST fields. When all fields are specified in an OP instruction, several different tasks are performed at once. The high five bits make up the OP field, summarized in table 1.

Table 2 summarizes the effect on bits in the PSW resulting from ALU operations.

Control Field [CNT]

This 12-bit field contains specifications for control modes and pointer modifications. Figure 5 summarizes the bit field format, table 3 summarizes the function of CNT field groups, and table 4 summarizes the function of each mnemonic within the 23 groups.

P Field

The two-bit P field specifies the source of input to the P register, which is used as an input to the ALU for operations requiring two operands. See table 5.

Figure 4. Instruction Type Formats

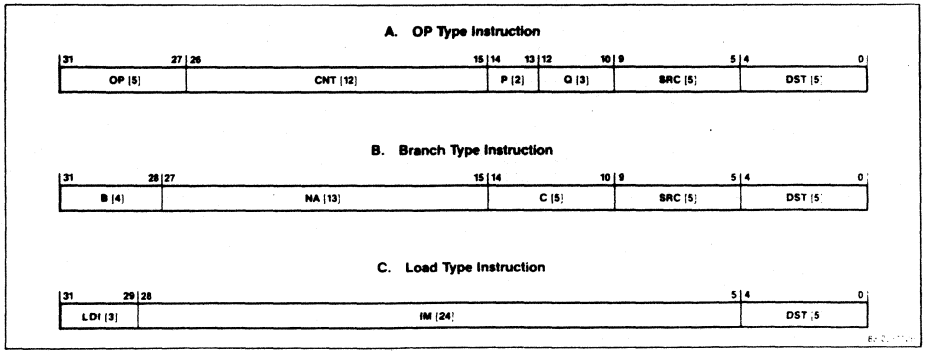


Table 1. OP Field Specifications

Mnemonic	OP Field (31-27)	Operation
NOP	00000	No operation
INC	00001	Increment
DEC	00010	Decrement
ABS	00011	Absolute value
NOT	00100	Not-one's complement
NEG	00101	Negate-two's complement
SHLC	00110	Shift left with carry
SHRC	00111	Shift right with carry
ROL	01000	Rotate left
ROR	01001	Rotate right
SHLM	01010	Shift left multiple
SHRM	01011	Shift right multiple
SHRAM	01100	Shift right arithmetic multiple
CLR	01101	Clear
NORM	01110	Normalize
CVT	01111	Convert floating point format
ADD	10000	Fixed-point add
SUB	10001	Fixed-point subtract
ADDC	10010	Fixed-point add with carry
SUBC	10011	Fixed-point subtract with borrow
CMP	10100	Compare (floating point)
AND	10101	Logical AND
OR	10110	Logical OR
XOR	10111	Logical exclusive OR
ADDF	11000	Floating-point add
SUBF	11001	Floating-point subtract

Table 2. Effects of ALU Operations on PSW Flags

ALU Operation	Contents of PSW				
	OVFE	C	Z	S	OVFM
NOP	*	*	*	*	*
INC	*	$	$	$	$
DEC	*	$	$	$	$
ABS	*	$	$	0	$+
NOT	*	0	$	$	0
NEG	*	$	$	$	$+
SHLC	*	$	$	$	0
SHRC	*	$	$	$	0
ROL	*	0	*	$	0
ROR	*	0	*	$	0
SHLM	*	0	$	$	0
SHRM	*	0	$	$	0

Table 2. Effects of ALU Operations on PSW Flags (cont)

ALU Operation	Contents of PSW				
	OVFE	C	Z	S	OVFM
SHRAM	*	0	$	$	0
CLR	0	0	1	0	0
NORM (NORM.)	$	0	$	$	0
(ROUNDING)	$	$	$	$	$
(FLT-FIX)	*	0	$	$	$
(FIX M.A.)	*	0	$	$	$
CVT	X	0	$	$	0
ADD	*	$	$	$	$
SUB	*	$	$	$	$
ADDC	*	$	$	$	$
SUBC	*	$	$	$	$
CMP	$	$	$	$	$
AND	*	0	$	$	0
OR	*	0	$	$	0
XOR	*	0	$	$	0
ADDF	$	$	$	$	$
SUBF	$	$	$	$	$

$ Flag will be affected by result of operation.

0 Flag will be reset to 0.

1 Flag will be reset to 1.

* Previous condition of flag will be preserved.

\+ If the original data in the mantissa was 80---0H, OVFM = 1 after operation.

Figure 5. Control Field Bit Format

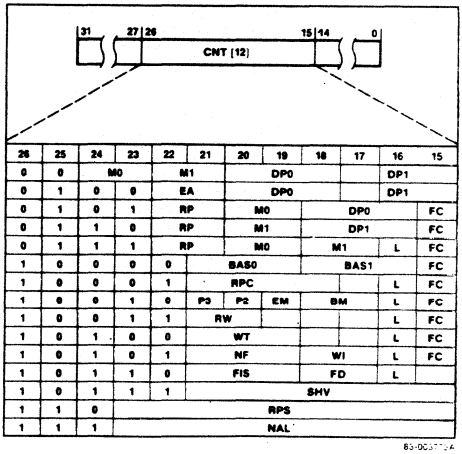


Table 3. Control Field Function Summary

Group	Field	Function	Effective
Interrupt	EM, BM	Enable and disable maskable interrupt, and control interrupt memorization.	→
PSW	FIS	PSW control (select and clear)	*
	FC	Select other PSW	*
Data ROM pointer	RP	Controls ROM pointer operation	→
	RPC	Specifies n value for special manipulation of ROM pointer	→
	RPS	Specifies 9 lower bits of data ROM address	→
Data RAM0 and RAM1 pointers	M0	Specifies RAM0 addressing mode	→
	M1	Specifies RAM1 addressing mode	→
	DP0	Controls modification of base pointer 0 and index register 0	→
	DP1	Controls modification of base pointer 1 and index register 1	→
	BASE0	Specifies counter length of modulo count operation of base pointer 0	→
	BASE1	Specifies counter length of modulo count operation of base pointer 1	→
Data format conversion	FD	Controls conversion mode for floating point CVT.	*
	WI	Controls transfer format when working register is specified in DST field.	→
	WT	Controls transfer format when working register is specified in SRC field.	→
Normalization specification	NF	Specifies normalization, normalization with rounding, floating-point to fixed-point conversion, or digit alignment.	*
Shift specification	SHV	Controls amount of shift for 47-bit mantissa	*
Data memory access	RW	Specifies read/write operation for external memory.	*
	EA	Increments or decrements external address register	*
General-purpose output port	P2	Controls state of P2 pin	→
	P3	Controls state of P3 pin	→
Loop counter	L	Decrements loop counter	→
Jump	NAL	Specifies unconditional local jump address	*

* Effective starting with current instruction.

→ Effective starting with next instruction.

Table 4. Control Field Mnemonic Summary

Operation	Mnemonic		Code
EM, BM Field (19-17)			
Maskable interrupt	EM	BM	
No operation	(NOP)	(NOP)	000
Clear booking flag	(NOP)	CLRBM	001
Set booking flag	(NOP)	SETBM	010
Interrupt disabled	DI	(NOP)	011
Interrupt enabled	EI	(NOP)	100
Interrupt enabled and clear booking flag	EI	CLRM	101
Interrupt enabled and set booking flag	EI	SETBM	110
Use prohibited	—	—	111
* Default: interrupt disabled and clear booking flag.			
* Writing (NOP) is not necessary, just useful for remembering the available combinations and their effects.			
FIS Field (21-19)			
Flag initialize and select			
No operation	(NOP)		000
Specify PSW 0 for operation (default)	SPCPSW0		001
Specify PSW 1 for operation	SPCPSW1		010
Clear PSW 0	CLRPSW0		100
Clear PSW 1	CLRPSW1		101
Clear PSW 0 and PSW 1	CLRPSW		110
FC Bit (15)			
Flag change operation			
No operation	(NOP)		0
Exchange PSW for operation	XCHPSW		1
RP Field (22, 21)			
ROM pointer modification			
No operation	(NOP)		00
Increment ROM pointer	INCRP		01
Decrement ROM pointer	DECRP		10
Increment specified bit of ROM pointer (that is, add 2^N)	INCBRP		11
RPC Field (21-18)			
Specify N for adding 2^N to ROM pointer	BITRP imm		(imm)B
*imm (= n) is 0 through 9			
RPS Field (23-15)			
Specify immediate ROM address	SPCRA imm		(imm)B
*$0 \leq imm \leq 511$			

Table 4. Control Field Mnemonic Summary (cont)

Operation	Mnemonic	Code
M0 Field		
Specify RAM pointer		
No change in specification	(NON)	00
Base pointer 0	SPCBP0	01
Index register 0	SPCIX0	10
Base pointer 0 + index register 0 (default)	SPCBI0	11
M1 Field		
Specify RAM pointer		
No change in specification	(NON)	00
Base pointer 1	SPCBP1	01
Index register 1	SPCIX1	10
Base pointer 1 + index register 1 (default)	SPCBI1	11
DP0 Field		
Pointer modification operation		
No operation	(NOP)	000
Increment base pointer 0	INCBP0	001
Decrement base pointer 0	DECBP0	010
Clear base pointer 0	CLRBP0	011
Store base + index to index register 0	STIX0	100
Increment index register 0	INCIX0	101
Decrement index register 0	DECIX0	110
Clear index register 0	CLRIX0	111
DP1 Field		
Pointer modification operation		
No operation	(NOP)	000
Increment base pointer 1	INCBP1	001
Decrement base pointer 1	DECBP1	010
Clear base pointer 1	CLRBP1	011
Store base + index to index register 1	STIX1	100
Increment index register 1	INCIX1	101
Decrement index register 1	DECIX1	110
Clear index register 1	CLRIX1	111
BASE0 Field (21-19)		
Specify modulo count number (2^N) for incrementing base pointer 0	MCNBP0 imm	(imm)B
*imm (=n) is 1 through 7; 0 specifies ordinary count		
BASE1 Field (18-16)		
Specify modulo count number (2^N) for incrementing base pointer 1	MCNBP1 imm	(imm)B
*imm (=n) is 1 through 7; 0 specifies ordinary count		

Operation	Mnemonic	Code
FD Field		
Data conversion format specification		
No change of specification	(NON)	00
Conversion of ASP format to IEEE format (default)	SPIE	01
Conversion of IEEE format to ASP format	IESP	10
Use prohibited		11
WI Field (18, 17)		
Specification of transfer format when data is moved from IB to WR		
No change of specification	(NON)	00
Transfer low 24 bits of mantissa to high 24 bits	BWRL24	01
Ordinary transfer (default)	BWRORD	10
Use prohibited		11
WT Field (21-19)		
Specification of transfer format when data is moved from WR to IB		
No change of specification	(NON)	000
Ordinary transfer (default)	WRBORD	001
Low 24 bits of mantissa to high 24	WRBL24	010
Low 23 bits (bit 23 = 0) to high 24	WRBL23	011
Exponent part to mantissa low 8 bits	WRBEL8	100
Mantissa low 8 bits to exponent part	WRBL8E	101
Exchange high 8 bits of mantissa with low 8 bits of mantissa	WRBXCH	110
Bit reverse entire mantissa	WRBBRV	111
NF Field (21-19)		
Normalization format specification		
No change of specification	(NON)	000
Truncating normalization (default)	TRNORM	010
Rounding normalization	RDNORM	100
Convert floating to fixed point	FLTFIX	110
Fixed point multiple alignment (multiple value is in SVR)	FIXMA	111
SHV Field (21-15)		
Set shift value to SVR		
imm bits left shift (default)	SETSVL imm	0 (imm)B
imm bits right shift	SETSVR imm	1 (imm)B
*0 ≤ imm ≤ 46		

Table 4. Control Field Mnemonic Summary (cont)

Operation	Mnemonic	Code
RW Field (21, 20)		
Operation for external data memory		
No operation	(NOP)	00
Read	RD	01
Write	WR	10
Use prohibited		11
EA Field (22, 21)		
Operation for external address register		
No operation	(NOP)	00
Increment external address register	INCAR	01
Decrement external address register	DECAR	10
Use prohibited		11
P2 Bit (20)		
P2 pin control (slave mode only)		
Clear output port pin 2	CLRP2	0
Set output port pin 2	SETP2	1
P3 Bit (21)		
P3 pin control (slave mode only)		
Clear output port pin 3	CLRP3	0
Set output port pin 3	SETP3	1
L Bit (16)		
Loop counter operation		
No operation	(NOP)	0
Decrement loop counter	DECLC	1
NAL Bit (23-15)		
Local branch; jump to imm address in local block	JBLK imm	(imm)B

*$0 \leq imm \leq 511$

Table 5. P Field Specifications

Mnemonic	P Field (14, 13)	Input of P Register
IB	00	Internal bus
M	01	Multiplier output register
RAM0	10	RAM block 0
RAM1	11	RAM block 1

Q Field

The three-bit Q field specifies the source of input to the Q register, which is the other of two ALU input registers. See table 6.

Table 6. Q Field Specifications

Mnemonic	Q Field (12-10)	Register
WR0	000	Working register 0
WR1	001	Working register 1
WR2	010	Working register 2
WR3	011	Working register 3
WR4	100	Working register 4
WR5	101	Working register 5
WR6	110	Working register 6
WR7	111	Working register 7

Source Field

Table 7 lists 32 source registers that may be specified in the source field.

Destination Field

Table 8 lists 32 destinations that may be specified in the DST field. Note that the LKR0 and KLR1 specifications will simultaneously load, as destinations, both the K and L registers.

Branch Instruction

The branch instruction type is used for a jump, conditional jump, call, or return. The format of the branch instruction is shown in figure 4. The destination address of the branch is contained in the 13-bit NA field. Note that the most significant bit of the NA field is used to determine whether the destination address is in internal or external instruction memory. The five-bit C field summarized in table 9 determines the nature of the branch.

Note also that an SRC and DST may be included as part of the branch instruction. This data transfer will take place regardless of any condition upon which a jump may be dependent.

LDI Instruction

Figure 4 shows the format of the LDI instruction type. The 24-bit IM (immediate) field contains the data that will be loaded into the register specified by the DST field. It is also possible to load a 32-bit floating-point number using this instruction in conjunction with the TRE destination field specification.

Table 7. SRC Field Specifications

Mnemonic	SRC Field (9-5)	Selected Source Register
NON	00000	No source selected
RP	00001	ROM pointer
PSW0	00010	Program status word 0
PSW1	00011	Program status word 1
SVR	00100	SVR (shift value register)
SR	00101	Status register
LC	00110	Loop counter
STK	00111	Top of stack
M	01000	M register (multiplier output)
ML	01001	Low 24 bits of M register
ROM	01010	Data ROM output
TR	01011	Temporary register
AR	01100	External address register
SI	01101	Serial input register
DR	01110	Data register
DRS	01111	Data register for slave
WR0	10000	Working register 0
WR1	10001	Working register 1
WR2	10010	Working register 2
WR3	10011	Working register 3
WR4	10100	Working register 4
WR5	10101	Working register 5
WR6	10110	Working register 6
WR7	10111	Working register 7
RAM0	11000	RAM block 0
RAM1	11001	RAM block 1
BP0	11010	Base pointer 0
BP1	11011	Base pointer 1
IX0	11100	Index register 0
IX1	11101	Index register 1
K	11110	K register
L	11111	L register

Table 8. DST Field Specifications

Mnemonic	DST Field (4-0)	Selected Destination Register
NON	00000	No destination selected
RP	00001	ROM pointer
PSW0	00010	Program status word 0
PSW1	00011	Program status word 1
SVR	00100	SVR (shift value register)
SR	00101	Status register
LC	00110	Loop counter
STK	00111	Top of stack
LKR0	01000	L register (RAM 0 to K register)
KLR1	01001	K register (RAM 1 to L register)
TRE	01010	Exponent part of temporary register
TR	01011	Temporary register
AR	01100	External address register
SO	01101	Serial output register
DR	01110	Data register
DRS	01111	Data register for slave
WR0	10000	Working register 0
WR1	10001	Working register 1
WR2	10010	Working register 2
WR3	10011	Working register 3
WR4	10100	Working register 4
WR5	10101	Working register 5
WR6	10110	Working register 6
WR7	10111	Working register 7
RAM0	11000	RAM block 0
RAM1	11001	RAM block 1
BP0	11010	Base pointer 0
BP1	11011	Base pointer 1
IX0	11100	Index register 0
IX1	11101	Index register 1
K	11110	K register
L	11111	L register

Table 9. Branch Condition Summary (C Field)

Mnemonic	C Field (14-10)	Jump with Condition
JMP	00000	Jump unconditionally
CALL	00001	Subroutine call
RET	00010	Return from interrupt or subroutine
JNZRP	00011	Jump if ROM pointer not zero
JZ0	00100	Jump if zero flag 0 is set
JNZ0	00101	Jump if zero flag 0 is reset
JZ1	00110	Jump if zero flag 1 is set
JNZ1	00111	Jump if zero flag 1 is reset
JC0	01000	Jump if carry flag 0 is set
JNC0	01001	Jump if carry flag 0 is reset
JC1	01010	Jump if carry flag 1 is set
JNC1	01011	Jump if carry flag 1 is reset
JS0	01100	Jump if sign flag 0 is set
JNS0	01101	Jump if sign flag 0 is reset
JS1	01110	Jump if sign flag 1 is set
JNS1	01111	Jump if sign flag 1 is reset
JV0	10000	Jump if overflow flag 0 is set
JNV0	10001	Jump if overflow flag 0 is reset
JV1	10010	Jump if overflow flag 1 is set
JNV1	10011	Jump if overflow flag 1 is reset
JEV0	10100	Jump if exponent overflow flag 0 is set
JEV1	10101	Jump if exponent overflow flag 1 is set
JNFSI	10110	Jump if SI register is not full
JNES0	10111	Jump if SO register is not empty
JIP0	11000	Jump if input port 0 is on
JIP1	11001	Jump if input port 1 is on
JNZIX0	11010	Jump if index register 0 nonzero
JNZIX1	11011	Jump if index register 1 nonzero
JNZBP0	11100	Jump if base pointer 0 nonzero
JNZBP1	11101	Jump if base pointer 1 nonzero
JRDY	11110	Jump if ready is on
JROM	11111	Jump if request for master is on

System Configurations

The μPD77230 may be configured in a variety of ways, from simple systems to complex. Figure 6 is the simplest example showing the μPD77230 as a stand-alone processor performing a preset filtering function. The only other devices needed are A/D and D/A converters, which can be a single-chip combo device as shown in the figure plus necessary clock and timing circuitry. Figure 7 shows the same stand-alone operation with external memory and memory-mapped I/O to implement various control functions along with processing the signal itself.

Figure 6. Stand-Alone μPD77230 with Codec

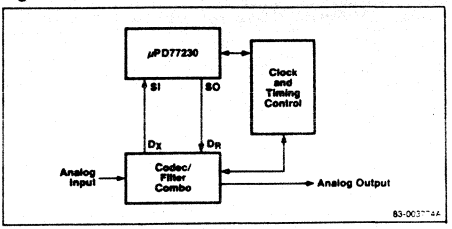


Figure 7. Stand-Alone μPD77230 with Codec, External Memory, and I/O

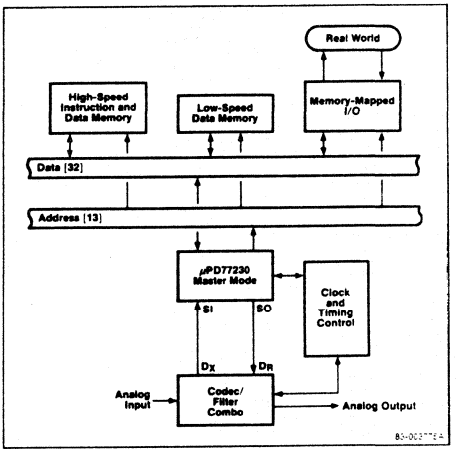


Figure 8 shows a μPD77230 in a slave mode as a peripheral to a host processor. Note that in slave mode, the μPD77230 can still be the "master" of its local bus with the four general purpose I/O pins available for use.

Figure 9 shows how to cascade multiple μPD77230s to increase system throughput. The cascading is done by using only the serial ports so that the μPD77230s themselves can be in any mode of operation desired. For example, they may all be in master mode, they may all be slaves to the same host processor, they may all be slaves to different hosts, or one may be the master with the others as slaves to it.

Figure 10 shows an arbitrarily large system with cascading master mode and slave mode μPD77230s. In this example, the master μPD77230 might do little actual signal processing. Instead, it will be an overall system controller gathering information from inputs in

the I/O block, from the slave μPD77230 I/O ports, and from its own processing of the signal. It will then control the other μPD77230s and the system outputs of the I/O block.

Support Tools

The μPD77230 has a wide variety of development and software support tools. Both absolute and relocatable assemblers, with powerful pre-assembler options, are available. In addition, a software simulator and in-circuit emulator will aid the designer in performance evaluation and hardware integration. The software tools options are as follows:

- Assembler: CP/M-86, VAX VMS, VAX UNIX
- Simulator: VAX VMS, VAX UNIX

Figure 8. Slave μPD77230 as Peripheral to Host Processor

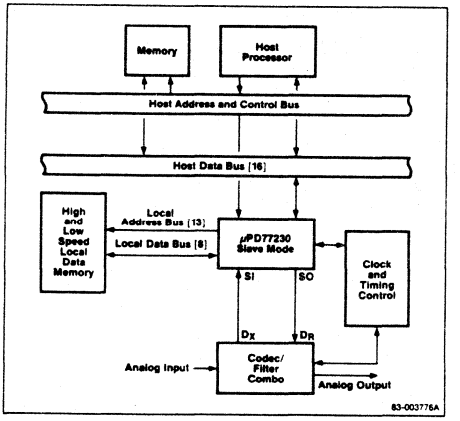


Figure 9. μPD77230s Cascaded Through Serial I/O Ports

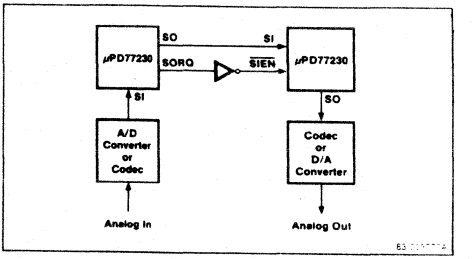
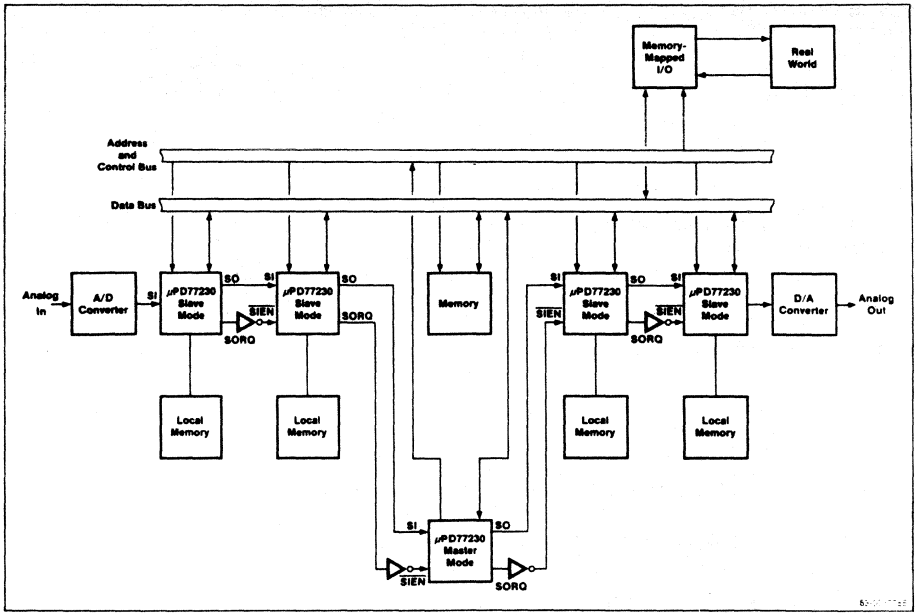


Figure 10. Large System with Many Options



Description

The μPD7730 speech encoder/decoder (SED) is a dedicated processor that encodes pulse coded modulation (PCM) data into adaptive differential pulse coded modulation (ADPCM) data, and decodes ADPCM data into PCM data. By using the ADPCM coding technique, the μPD7730 effectively reduces the bandwidth of a speech signal to less than half that of the conventional PCM method without sacrificing speech quality.

The μPD7730 accepts PCM data through its serial interface. The serial interface can be connected directly to a single-chip coder/decoder (CODEC) for digital μ-law PCM I/O or to a general purpose A/D-D/A converter for linear PCM code. The μPD7730 interfaces to the host CPU through a standard microprocessor bus interface. The μPD7730 acts as a complex peripheral device and is controlled and programmed from the host processor. ADPCM data is transferred between the μPD7730 and the host processor through the parallel bus.

The μPD7730 encodes/decodes toll quality speech at 32 kbps. It integrates NEC's speech coding expertise with a high-performance signal processor. It is ideal for office automation applications, such as voice store and forward systems, and for various telecommunication applications. It reduces voice transmission bandwidth and voice storage requirements by half (from 64 kbps to 32 kbps).

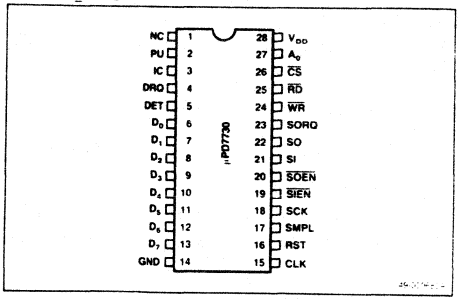
Features

- ☐ Toll quality speech at 32 kbps (meets CCITT recommendation G.712)
- ☐ Program selectable bit rate: 32 kbps or 24 kbps
- ☐ Program selectable PCM data format: μ-law or linear
- ☐ Standard microprocessor interface to the host CPU
- ☐ Direct serial interface to a CODEC
- ☐ Speech detection interface capability
- ☐ NMOS technology
- ☐ Single +5 V power supply

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7730C	28-pin plastic DIP	8.192

Pin Configuration



Pin Identification

No.	Symbol	Function
1	NC	No connection
2	PU	Pull up to V_{DD}
3	IC	Internal connection
4	DRQ	Data request output
5	DET	Signal detect output
6-13	D_0-D_7	I/O data bus
14	GND	Ground
15	CLK	Clock input
16	RST	Reset input
17	SMPL	Sample input
18	SCK	Serial clock input
19	$\overline{SIEN}$	Inputs serial input enable
20	$\overline{SOEN}$	Inputs serial output enable
21	SI	Serial input
22	SO	Serial output
23	SORQ	Serial output request
24	$\overline{WR}$	Write signal input
25	$\overline{RD}$	Read signal input
26	$\overline{CS}$	Chip select input
27	A_0	Register select input
28	V_{DD}	Power supply

Pin Functions

D_0-D_7 (Data Bus)

Three-state I/O lines that interface with the host CPU data bus.

$\overline{CS}$ (Chip Select)

This input enables the RD and WR signals.

A_0 (Register Select)

This input selects the μPD7730 internal registers. A high input selects the status register. A low input selects the data register.

DRQ (Data Request)

This output requests data transfer between the μPD7730 and host CPU. In encoder mode, an ADPCM data read is requested. In decoder mode, an ADPCM data write is requested. (DRQ will not work unless encoder or decoder mode is specified.) The data request status can also be checked by polling the RQM bit of the status register.

DET (Signal Detect)

This output is asserted when the input audio signal level exceeds the threshold level specified.

$\overline{WR}$ (Write Signal)

This input controls data transfer from the host CPU to the μPD7730.

$\overline{RD}$ (Read Signal)

This input controls data transfer from the μPD7730 to the host CPU.

SMPL (Sample)

This input determines the rate at which the μPD7730 processes ADPCM data. This rate must equal the sampling clock of the A/D-D/A converter. SMPL must be active for the μPD7730 to recognize an operation command.

SCK (Serial Clock)

This input provides timing for transfer of serial data to/from the A/D-D/A converter.

SI (Serial Input)

Serial data input.

$\overline{SIEN}$ (Serial Input Enable)

This input enables data transfer on the SI pin. If not used, tie to $\overline{SOEN}$. $\overline{SIEN}$ must be asserted for the μPD7730 to recognize an operation command.

SO (Serial Output)

Serial data output.

SORQ (Serial Output Request)

This output indicates that serial request output data is ready for transfer at the SO pin.

$\overline{SOEN}$ (Serial Output Enable)

This input enables data transfer on the SO pin. If not used, tie to $\overline{SIEN}$.

CLK (Clock)

8.192 MHz TTL clock input.

RST (Reset)

A high input to this pin initializes the μPD7730.

V_{DD}

+5 V power supply.

PU (Pull up)

Pull this pin up to V_{DD}.

GND (Ground)

Connection to ground.

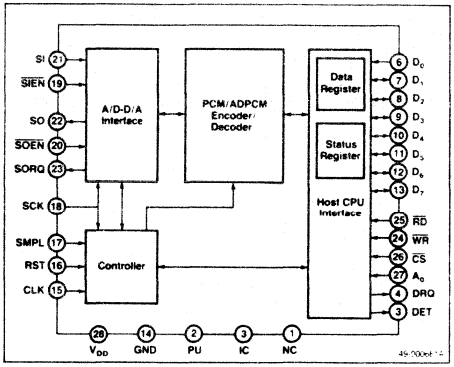
IC (Internal Connection)

This pin is connected internally and should be left open.

NC (No Connection)

This pin is not connected.

Block Diagram



Functional Description

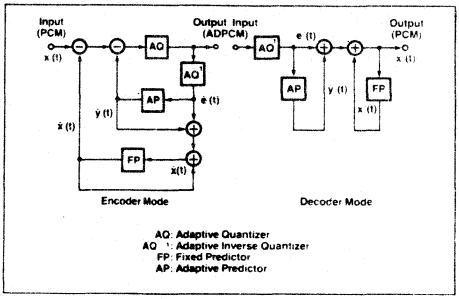
The μPD7730 has the following functional units:

- A/D-D/A interface
- PCM/ADPCM encoder/decoder
- Controller
- Data register
- Status register
- Host CPU interface

The ADPCM method is a medium bandwidth coding technique that represents speech waveforms. The specific ADPCM used employs a robust adaptation scheme for a quantizer and predictor to withstand transmission bit errors. Figure 1 shows the block diagram of the algorithm. The algorithm uses a backward adaptive quantizer and a fixed predictor so it never generates unstable poles in a decoder transfer function. This approach guarantees the stability of the decoder even with transmission errors.

The μPD7730 can operate in either encoder or decoder mode, and can only be set to one of the two modes at a time; it cannot handle simultaneous encoding and decoding. In encoder mode, the μPD7730 accepts either linear or μ-law PCM data from its serial voice interface, encodes it to ADPCM data format, and passes the ADPCM data through the parallel data bus to the host system. In decoder mode, the μPD7730 receives ADPCM data from the host CPU, decodes it to either linear or μ-law format, and sends it to the output port of the serial interface.

Figure 1. Algorithm Block Diagram



The μPD7730 has serial interfaces that can connect directly to a single-chip PCM CODEC. It interfaces easily to a host CPU through its parallel bus. With its standard microprocessor bus interface, the μPD7730 can be viewed as a complex peripheral circuit. Figure 2 shows a typical system configuration.

Operational Description

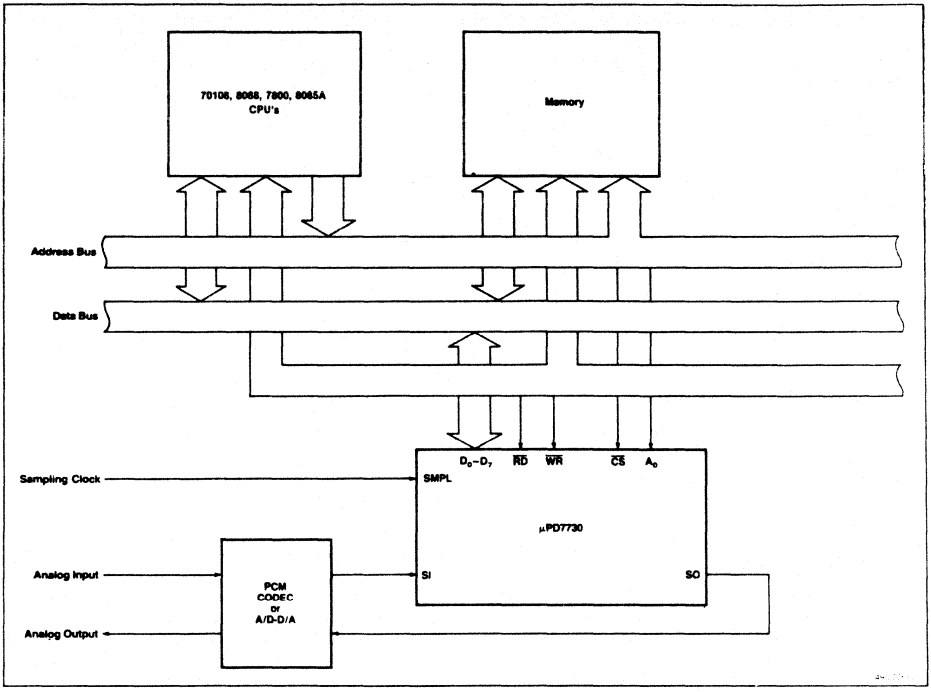
Power-on and Reset

The μPD7730 operates on a single-phase, 50-50 duty cycle clock at 8 MHz. At power-on, asserting the RST pin for at least 3 clock cycles initializes the device, making it ready for an operation command from the host CPU. After the μPD7730 receives the command, it stays in the specified operational mode until the next hardware reset (high level on RST). Thus, to change the μPD7730 into different modes, reset it before writing an operation command.

Host CPU Interface

In order to transfer ADPCM data, commands, and status, the μPD7730 interfaces with the host CPU via D_0-D_7. Further communication is through control lines $\overline{CS}$, A_0, $\overline{WR}$, and $\overline{RD}$. $\overline{CS}$ enables $\overline{RD}$ and $\overline{WR}$. A_0 selects either the data or status register. A low input to A_0 selects the data register. This read/write register handles both commands and ADPCM data transfer. A high input to A_0 selects the status register, a read-only register that the CPU reads to determine the state of the μPD7730.

Figure 2. Typical System Configuration



Parallel I/O Operation

Table 1 shows the status of the $\overline{CS}$, A_0, $\overline{WR}$, and $\overline{RD}$ pins during parallel I/O operation.

Status Register

Figure 3 shows the format of the status register.

Operation Command

Following a power-on reset, the host CPU polls the RQM bit in the status register. When the RQM bit is set, the host CPU can send an operation command to the data register, as shown in figure 4.

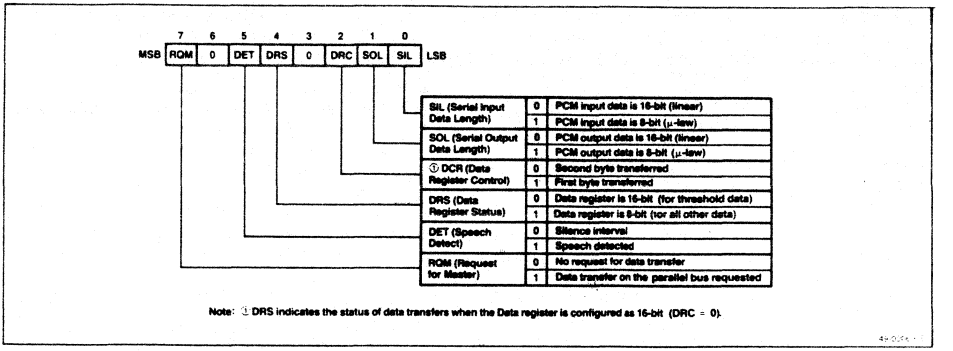
Table 1. Control Line States

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Function
1	X	X	X	No effects on internal operation.
X	X	1	1	D_0–D_7 are high impedance.
0	0	0	1	Data from D_0–D_7 is latched to the data register.
0	0	1	0	Contents of the data register are output to D_0–D_7.
0	1	0	1	Illegal operation.
0	1	1	0	Contents of the status register are output to D_0–D_7.

Note:

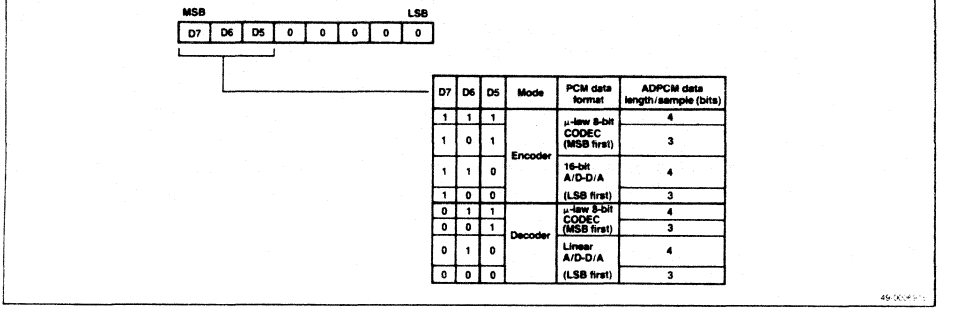
X = don't care

Figure 3. Status Register Format



Note: ① DRS indicates the status of data transfers when the Data register is configured as 16-bit (DRC = 0).

Figure 4. Operation Command



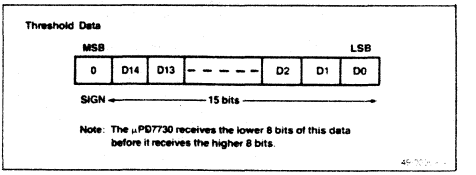
D7	D6	D5	Mode	PCM data format	ADPCM data length/sample (bits)
1	1	1	Encoder	μ-law 8-bit CODEC (MSB first)	4
1	0	1			3
1	1	0		16-bit A/D-D/A	4
1	0	0		(LSB first)	3
0	1	1	Decoder	μ-law 8-bit CODEC (MSB first)	4
0	0	1			3
0	1	0		Linear A/D-D/A	4
0	0	0		(LSB first)	3

Threshold Data

If the operation command places the μPD7730 in encoder mode, the next two bytes sent to the data register are the threshold data. The RQM bit establishes the data transfer signaling. In decoder mode, no threshold data is expected. The threshold data sets the level of the audio signal at which the DET pin is asserted. Figure 5 shows the format for the threshold data.

The μPD7730 asserts DET when the serial input audio signal exceeds the threshold level specified by the threshold data. Many silent segments exist in normal speech signals; memory storage can be used more efficiently if these segments are omitted. The host CPU can perform silent segment compression by using DET. The energy levels of 16 previous audio samples determine the state of DET. Thus DET changes at a 2 ms (16 x 8 kHz sampling) time frame. Bit 5 of the status register reflects the state of DET.

Figure 5. Threshold Data



Note: The μPD7730 receives the lower 8 bits of this data before it receives the higher 8 bits.

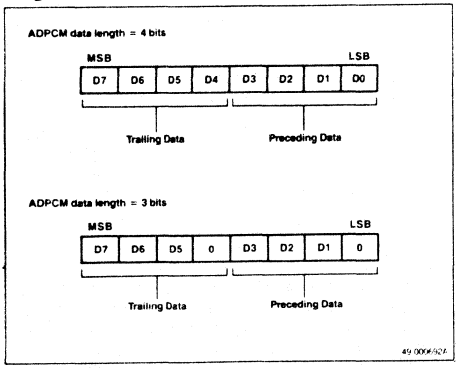
ADPCM Data

In encoder mode, the μPD7730 generates one ADPCM sample (3 or 4 bits long) for each PCM sample input (8 or 16 bits long). In decoder mode, the reverse operation is performed: the μPD7730 generates one PCM sample for each ADPCM sample input. To allow efficient data transfer to and from the host CPU, two ADPCM samples are packed into one byte and transferred at the rate of 1 byte per every 2 samples. Figure 6 illustrates the ADPCM data formats for 3 bits/sample and 4 bits/samples.

The DRQ pin initiates ADPCM data transfer. In encoder mode, this pin is asserted when ADPCM data in the data register is ready to be read by the CPU. This pin is cleared after the host CPU reads the data, and is reasserted when the next byte of ADPCM data becomes available. In decoder mode, this pin serves as the data request to the host for the next byte of ADPCM data to be sent to the data register. After the host CPU writes the ADPCM data, this pin is cleared. The host CPU cannot send another byte to the μPD7730 until this pin is set again. (Note that the DRQ pin will not work until the μPD7730 is placed in encoder or decoder mode.)

An alternate way to establish the ADPCM data transfer handshake is to poll the RQM bit in the status register. The RQM bit is set when transfer to the host is requested for ADPCM data, and in using the operation command. When the host read/write is complete, RQM is reset.

Figure 6. ADPCM Data Format



Serial PCM Interface

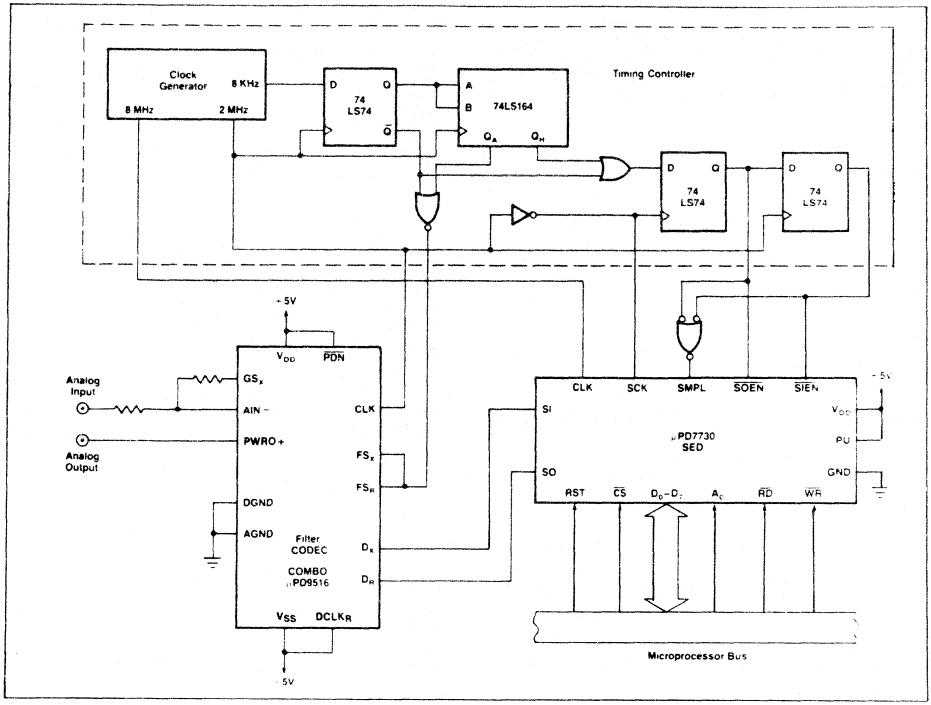
The serial PCM interface can be connected directly to a CODEC. SMPL, SCK, $\overline{SIEN}$, SI, SORQ, $\overline{SOEN}$, and SO control the PCM interface.

SMPL is the sampling clock input. This signal must equal the frequency of the sampling clock of the CODEC or the A/D-D/A interface. SMPL is asserted after the completion of serial data transfers. Thus SMPL signals the μPD7730 firmware to initiate processing of the next byte of ADPCM data. SMPL is rising-edge triggered, but must be held high for at least 8 clock cycles. Since it is edge-triggered, SMPL does not need to be released until the next sampling cycle.

SCK determines the timing of the serial input and output. When the μPD7730 has data to send to the serial interface, SORQ goes high. The data is then clocked out to the SO pin serially at the falling edge of SCK, to be valid for the next rising edge. When serial data is ready to be sent to the μPD7730, $\overline{SIEN}$ is asserted externally, and data at the SI pin is clocked in at the rising edge of SCK.

Figure 7 illustrates an example of the serial interface using a combined filter and CODEC (COMBO) chip, the μPD9516. This chip provides both the low pass filtering function and the conversion from an analog signal to digital PCM μ-law representation. The timing controller provides the proper timing relationship between the COMBO and the μPD7730.

Figure 7. Serial Interface Using a COMBO



Absolute Maximum Ratings*

T_A = 25°C

Supply voltage, V_{DD}	−0.5 V to +7.0 V
Input voltage, V_I	−0.5 V to +7.0 V
Output voltage, V_O	−0.5 V to +7.0 V
Operating temperature	−10°C to +70°C
Storage temperature	−65°C to +150°C

***Comment:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, V_{DD} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK, SCK capacitance	C_ϕ			20	pF	
Input capacitance	C_I			10	pF	fc = 1 MHz
Output capacitance	C_O			20	pF	

DC Characteristics

T_A = −10°C to +70°C; V_{DD} = +5 V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.5		0.8	V	
Input voltage high	V_{IH}	2.0		V_{CC} +0.5	V	
CLK input voltage low	$V_{\phi L}$	−0.5		0.45	V	
CLK input voltage high	$V_{\phi H}$	3.5		V_{CC} +0.5	V	
Output voltage low	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output voltage high	V_{OH}	2.4			V	I_{OH} = −400 μA
Input leakage current low	I_{LIL}			−10	μA	V_I = 0 V
Input leakage current high	I_{LIH}			10	μA	V_I = V_{DD}
Output leakage current low	I_{LOL}			−10	μA	V_O = 0.47 V
Output leakage current high	I_{LOH}			10	μA	V_O = V_{DD}
Supply current	I_{DD}		180	280	mA	

AC Characteristics

T_A = −10°C to +70°C; V_{DD} = 5 V ±5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK cycle time	$t_{\phi CY}$	122		2000	ns	
CLK pulse width	$t_{\phi D}$	60			ns	
CLK rise time	$t_{\phi r}$			10	ns	(1)
CLK fall time	$t_{\phi f}$			10	ns	(1)
A_0, $\overline{CS}$ set time for $\overline{RD}$	t_{AR}	0			ns	
A_0, $\overline{CS}$ hold time for $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ pulse width	t_{RR}	250			ns	
A_0, $\overline{CS}$ set time for $\overline{WR}$	t_{AW}	0			ns	
A_0, $\overline{CS}$ hold time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ pulse width	t_{WW}	250			ns	
Data set time for $\overline{WR}$	t_{DW}	150			ns	
Data hold time for $\overline{WR}$	t_{WD}	0			ns	
$\overline{RD}$, $\overline{WR}$ recovering time	t_{RV}	250			ns	
SCK cycle time	t_{SCY}	480		DC	ns	
SCK pulse time	t_{SCK}	230			ns	
SCK rise time	t_{rSC}			20	ns	
SCK fall time	t_{fSC}			20	ns	

AC Characteristics (cont)

T_A = −10°C to +70°C; V_{DD} = 5 V ±5%

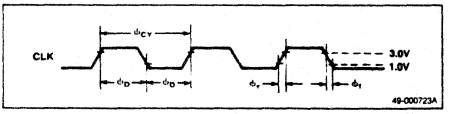
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SOEN}$ set time for SCK	t_{SOC}	50		t_{SCY} −30	ns	
$\overline{SOEN}$ hold time for SCK	t_{CSO}	30		t_{SCY} −50	ns	
$\overline{SIEN}$, SI set time for SCK	t_{DC}	55		t_{SCY} −30	ns	
$\overline{SIEN}$, SI hold time for SCK	t_{CD}	30		t_{SCY} −55	ns	
$\overline{SIEN}$, $\overline{SOEN}$ pulse width high	t_{HS}	122		$t_{\phi CY}$		
RST pulse width	t_{RST}	4		$t_{\phi CY}$		
SMPL pulse width	t_{SMPL}	8		$t_{\phi CY}$		
Delay time between SMPL and $\overline{SIEN}$ ($\overline{SOEN}$)	t_{DX}	−1	0	1	μs	
Data access time for $\overline{RD}$	t_{RD}			150	ns	C_L = 100 pF
Data float time for $\overline{RD}$	t_{DF}	10		100	ns	C_L = 100 pF
SORQ delay	t_{DRQ}	30		150	ns	C_L = 50 pF
SO delay time	t_{DCK}			150	ns	
SO delay time for SORQ	t_{DZRQ}	20		300	ns	
SO delay time for SCK	T_{DZSC}	20		300	ns	
SO delay time for $\overline{SOEN}$	t_{DZE}	20		180	ns	
SO float time for $\overline{SOEN}$	t_{HZE}	20		200	ns	
SO float time for SCK	t_{HZSC}	20		300	ns	
SO float time for SORQ	t_{HZRQ}	70		300	ns	

Note:

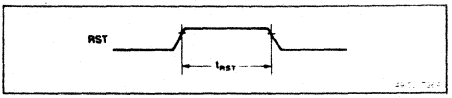
(1) AC timing measuring point voltage = 1.0 V and 3.0 V

Timing Waveforms

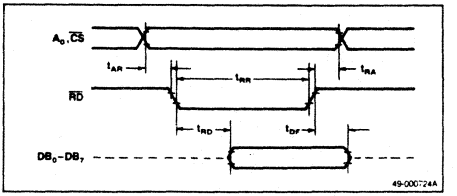
Clock



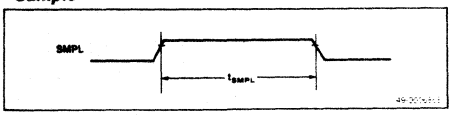
Reset



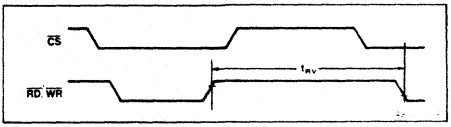
Read Operation



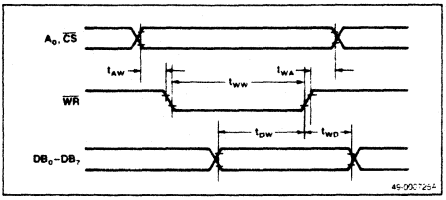
Sample



Read/Write Cycle Timing

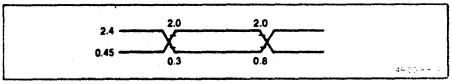


Write Operation



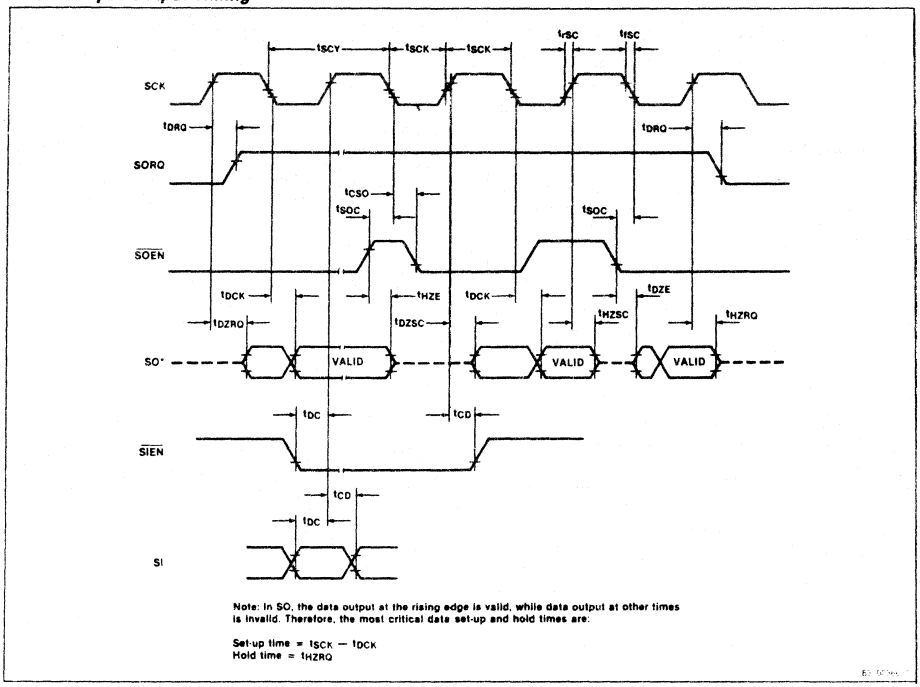
AC Waveform Measurement Points (except CLK)

$V_{IL} = V_{OL} = 0.8$ V; $V_{IH} = V_{OH} = 2.0$ V



Timing Waveforms (cont)

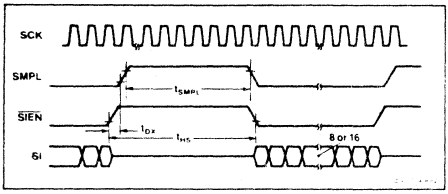
Serial Input/Output Timing



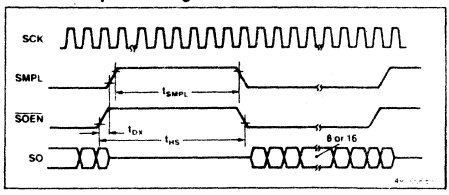
Note: In SO, the data output at the rising edge is valid, while data output at other times is invalid. Therefore, the most critical data set-up and hold times are:

Set-up time = $t_{SCK} - t_{DCK}$
Hold time = t_{HZRQ}

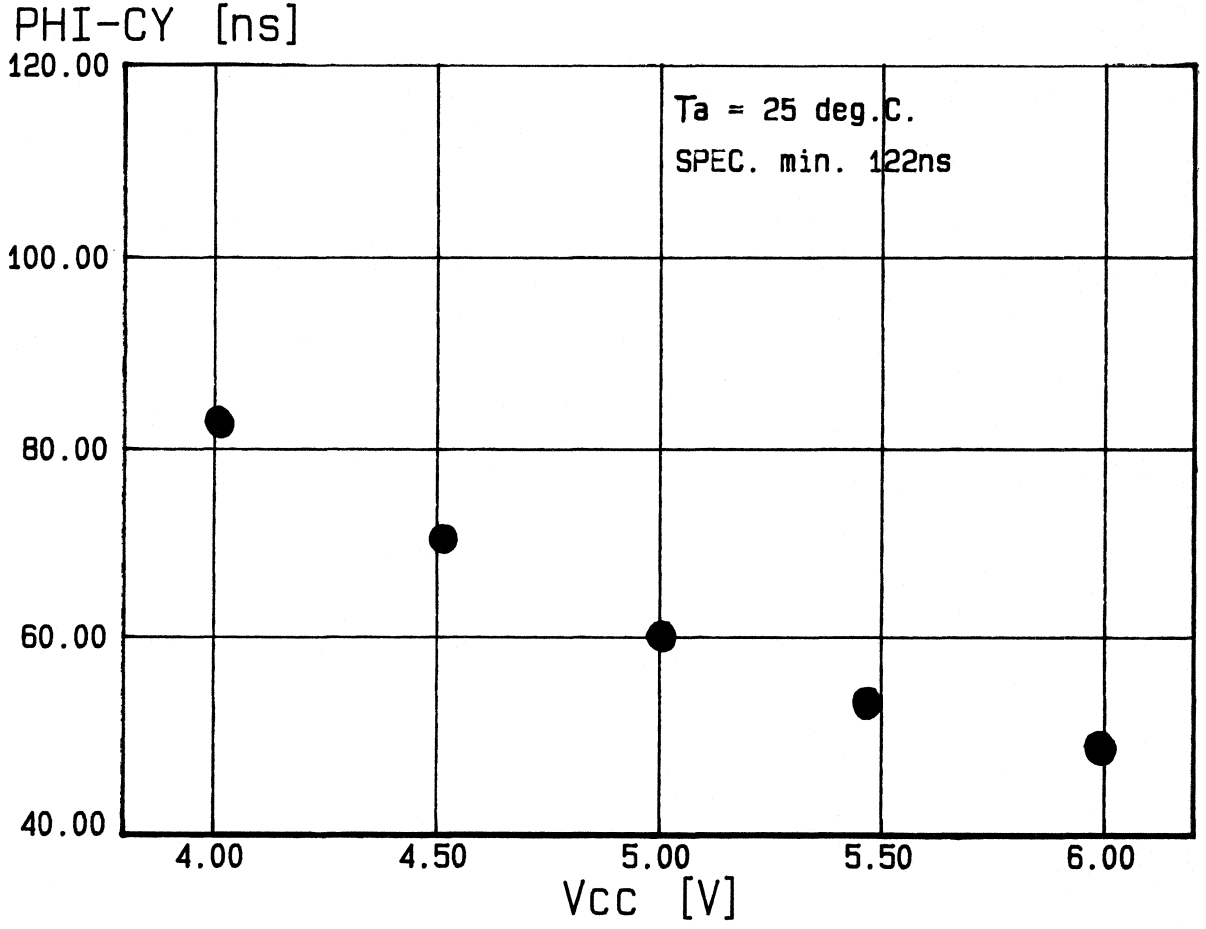
Serial Input Timing



Serial Output Timing



UPD77C20A CLOCK vs. SUPPLY VOLTAGE



Description

The μPD7755 and μPD7756 are speech synthesis LSI devices that utilize the adaptive differential pulse coded modulation (ADPCM) coding method to produce high-quality, natural speech synthesis. By combining phoneme classification with the ADPCM method, the device achieves a compressed bit rate that can synthesize sound effects and melodies in addition to speech sound. A built-in speech data ROM allows synthesis of messages up to 12 seconds (μPD7755) or 30 seconds (μPD7756) long. A wide range of operating voltages, a compact package, and a standby function permit application of the μPD7755/56 in a variety of speech synthesis systems, including battery-driven systems.

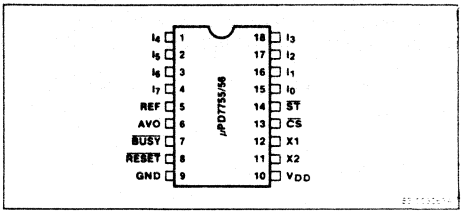
Features

- ☐ High quality speech synthesis using ADPCM method
- ☐ Low bit rates (8K to 32K bps) realized by combined use of ADPCM and phoneme methods
- ☐ D/A converter with 9-bit resolution, unipolar current waveform output
- ☐ Built-in speech data ROM,
  - — μPD7755: 96K bits
  - — μPD7756: 256K bits
- ☐ Standby function
- ☐ Current consumption in standby mode: 1 μA typ (V_{DD} = 3 V)
- ☐ Circuit to eliminate popcorn noise when entering or releasing standby mode
- ☐ Wide operating voltage range: 2.7 to 5.5 V
- ☐ CMOS technology
- ☐ 18-pin plastic DIP

Ordering Information

Part Number	Package Type	ROM Capacity	Max Frequency of Operation
μPD7755C	18-Pin plastic DIP	96K bits	650 kHz
μPD7756C	18-Pin plastic DIP	256K bits	650 kHz

Pin Configuration



Pin Identification

No.	Symbol	Name
15-18, 1-4	I_0-I_7	Message select code input
5	REF	D/A converter reference current input
6	AVO	Analog voice output
7	$\overline{BUSY}$	Busy output
8	$\overline{RESET}$	Reset input
9	GND	Ground
10	V_{DD}	Power
11, 12	X2, X1	Clock
13	$\overline{CS}$	Chip select input
14	$\overline{ST}$	Start input

Pin Functions

I_0-I_7 [Message Select Code]

I_0-I_7 input the message number of the message to be synthesized. The inputs are latched at the rising edge of the $\overline{ST}$ input. Unused pins should be grounded. In standby mode, these pins should be set high or low. If they are biased at or near typical CMOS switch input, they will drain excess current.

$\overline{CS}$ [Chip Select]

When the $\overline{CS}$ input goes low, $\overline{ST}$ is enabled.

$\overline{ST}$ [Start]

Setting the $\overline{ST}$ input low while $\overline{CS}$ is low will start speech synthesis of the message in the speech ROM locations addressed by the contents of I_0-I_7. If the device is in standby mode, standby mode will be released.

$\overline{\text{BUSY}}$ [Busy]

$\overline{\text{BUSY}}$ outputs the status of the μPD7755/56. It goes low during speech decode and output operations. When $\overline{\text{ST}}$ is received, $\overline{\text{BUSY}}$ goes low. While $\overline{\text{BUSY}}$ is low, another $\overline{\text{ST}}$ will not be accepted. In standby mode, $\overline{\text{BUSY}}$ becomes high impedance. This is an active low output.

AVO [Analog Voice Output]

AVQ outputs synthesized speech from the D/A converter. This is a unipolar sink-load current.

$\overline{\text{RESET}}$ [Reset]

The $\overline{\text{RESET}}$ input initializes the chip. Use $\overline{\text{RESET}}$ following power-up to abort speech synthesis or to release standby mode. $\overline{\text{RESET}}$ must remain low at least 12 oscillator clocks. At power-up or when recovering from standby mode, $\overline{\text{RESET}}$ must remain low at least 12 more clocks after clock oscillation stabilizes.

X1, X2 [Clock]

Pins X1 and X2 should be connected to a 640 kHz ceramic oscillator. In standby mode, X1 goes low, and X2 goes high.

REF [D/A Converter Reference Current]

REF inputs the sink-load current that controls the D/A converter output. REF should be connected to V_{DD} via a resistor. In standby mode, REF becomes high impedance.

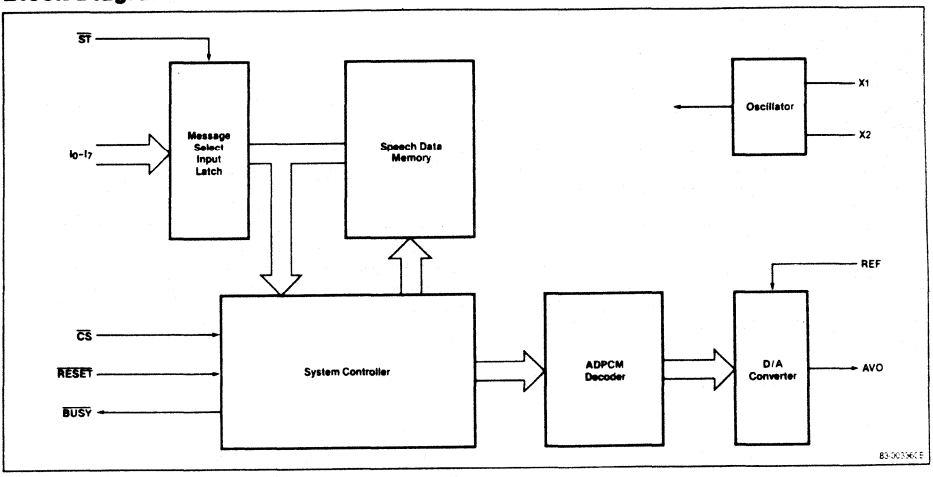
GND [Ground]

Ground.

V_{DD} [Power]

+5 V power supply.

Block Diagram



Operational Description

The clock pins should be connected to a ceramic oscillator at 640 kHz.

The $\overline{RESET}$ input pin is used to initialize the μPD7755/56. To reset, assert the pin for a minimum of 12 oscillator clock cycles.

The μPD7755/56 can operate with a wide range of supply voltages: 2.7 to 5.5 V. It also has a standby function; it goes to a standby mode when it has been idle (that is, when $\overline{CS}$, $\overline{ST}$, or $\overline{RESET}$ have not been asserted) for more than 3 seconds. The μPD7755/56 will automatically release from standby mode when $\overline{CS}$ and $\overline{ST}$ are asserted again, or when $\overline{RESET}$ is asserted.

The μPD7755/56 has a very simple message selection interface. A μPD7755/56 can store a maximum of 256 different messages and up to 12 (μPD7755) or 30 (μPD7756) seconds of speech. The message is selected by using the input pins I_0-I_7. The input selection is latched at the rising edge of $\overline{ST}$ when $\overline{CS}$ is asserted. When $\overline{ST}$ is asserted, $\overline{BUSY}$ will go low until the selected audio speech output is completed. While $\overline{BUSY}$ is low, a new $\overline{ST}$ will not be accepted.

The μPD7755/56 has an internal D/A converter that is a unipolar, current-output type with 9-bit resolution. The output current of the D/A can be controlled by the voltage applied at the REF pin.

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−40 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input pin capacitance	C_I			10	pF	fc = 1 MHz
Output pin capacitance	C_O			20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{DD} = 2.7 to 5.5 V; f_{osc} = 640 kHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH}	0.7 V_{DD}		V_{DD}	V	Common to I_0-I_7, $\overline{ST}$, $\overline{CS}$, $\overline{RESET}$
Input voltage low	V_{IL}	0		0.3 V_{DD}	V	Common to I_0-I_7, $\overline{ST}$, $\overline{CS}$, $\overline{RESET}$
Output voltage high	V_{OH}	V_{DD} −0.5		V_{DD}	V	$\overline{BUSY}$. I_{OH} = −100 μA
Output voltage low	V_{OL}	0		0.5	V	$\overline{BUSY}$. I_{OL} = 200 μA
Input leakage current	I_{LI}			±3	μA	Common to I_0-I_7, $\overline{ST}$, $\overline{CS}$. 0 ≤ V_{IN} ≤ V_{DD} (in standby mode)
Output leakage current	I_{LO}			±3	μA	$\overline{BUSY}$. 0 ≤ V_O ≤ V_{DD} (in standby mode)
Supply current	I_{DD1}		0.8	2	mA	—
	I_{DD2}		1	20	μA	Standby mode
	I_{DD3}		250	600	μA	2.7 ≤ V_{DD} ≤ 3.3
	I_{DD4}		1	10	μA	2.7 ≤ V_{DD} ≤ 3.3 in standby mode
Reference input high current area (1)	I_{REF1}	140	250	440	μA	V_{DD} = 2.7, R_{REF} = 0 Ω
	I_{REF2}	500	760	1200	μA	V_{DD} = 5.5, R_{REF} = 0 Ω
Reference input low current area (1)	I_{REF3}	21	35	37	μA	V_{DD} = 2.7, R_{REF} = 50 kΩ
	I_{REF4}	68	78	88	μA	V_{DD} = 5.5 V, R_{REF} = 50 kΩ
D/A converter output current (1)	I_{AVO}	$32I_{REF}$	$34I_{REF}$	$36I_{REF}$	μA	2.7 ≤ V_{DD} ≤ 5.5, V_{AVO} = 2.0, D/A input = 1FFH
D/A converter output leakage current	I_{LA}			±5	μA	0 ≤ V_{AVO} ≤ V_{DD}

Note:

(1) See figure 1.

AC Characteristics

$T_A = -10°$ to $+70°C$; $V_{DD} = 2.7$ to 5.5 V; $f_{osc} = 640$ kHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{ST}$ pulse width	t_{CC1}	2			μs	
	t_{CC2}	350			ns	$4.5 < V_{DD} < 5.5$
Data set time	t_{DW1}	2			μs	
	t_{DW2}	350			ns	$4.5 < V_{DD} < 5.5$
Data hold time	t_{WD}	0			ns	
$\overline{CS}$ set-up time	t_{CS}	0			ns	
$\overline{CS}$ hold time	t_{SC}	0			ns	
CLK frequency	f_{OSC}	630	640	650	kHz	
$\overline{BUSY}$ output time (from $\overline{ST}$ and/or $\overline{CS}$)	t_{SBO}		6.25	10	μs	Operation mode
	t_{SBS}		4	80	ms	Standby mode, including oscillation start time(1)
Speech output start time	t_{SSO}		2.1	2.2	ms	Operation mode (from $\overline{BUSY}$)
	t_{SSS}		2.1	2.2	ms	Standby mode
D/A converter set-up time	t_{DA}		46.5	47	ms	Entering/ releasing standby mode
$\overline{BUSY}$ float time	t_{BF}			15	μs	From end of speech output
Standby transition time	t_{STB}		2.9	3	s	From end of speech output

Note:

(1) Ceramic resonators: Kyocera Corp. KBR-640B (C1 = C2 = 150 pF). See figure 2.

AC Waveform Measurement Points

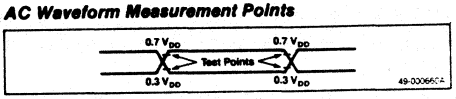


Figure 1. Measuring Diagram for I_{REF} and I_{AVO}

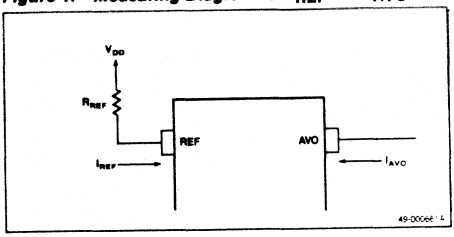
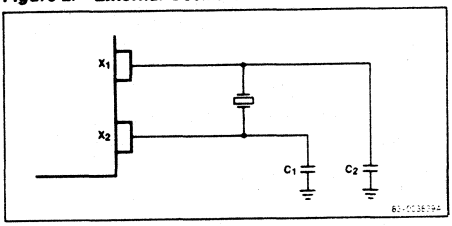
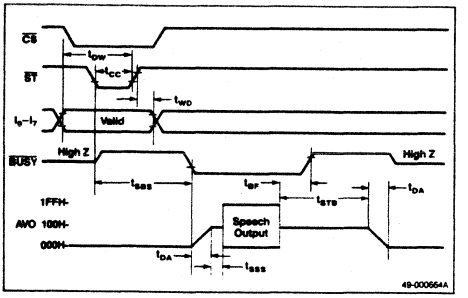


Figure 2. External Oscillator

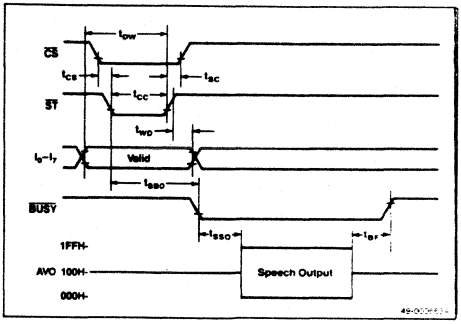


Timing Waveforms

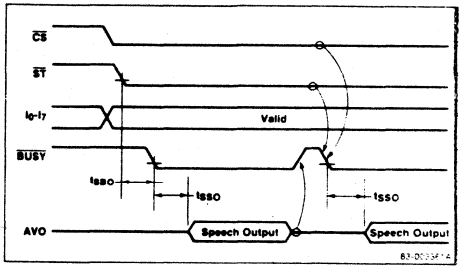
Standby Mode



Operating Mode (ST Input Pulse Mode)



Operating Mode (ST Input Hold Low Mode)



Description

The μPD7759 is a speech synthesis device that utilizes the adaptive differential pulse coded modulation (ADPCM) coding method to produce high-quality, natural speech synthesis. By combining phoneme classification with the ADPCM method, the device achieves a compressed bit rate that can synthesize sound effects and melodies in addition to speech sound. The μPD7759 can directly address up to 1M bits of external data ROM, or the host CPU can control the speech data transfer. The μPD7759 is also suitable for applications requiring small production quantities, long synthesized messages, and for emulating the μPD7755/7756.

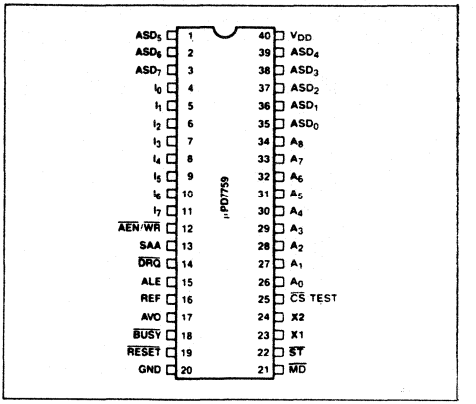
Features

- ☐ High-quality speech synthesis using ADPCM method
- ☐ Low bit-rates (8 to 32 kb/s) realized by combined use of ADPCM and phoneme methods
- ☐ D/A converter with 9-bit resolution, unipolar current waveform output
- ☐ Up to 1M bits addressing for external data ROM
- ☐ Standby function
- ☐ Circuit to eliminate popcorn noise when entering or releasing standby mode
- ☐ Wide operating voltage range: 2.7 to 5.5 V
- ☐ CMOS technology

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7759C	40-pin plastic DIP	650 kHz

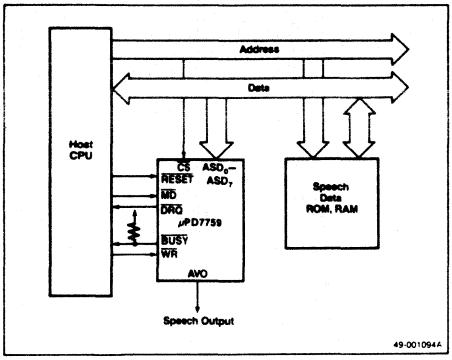
Pin Configuration



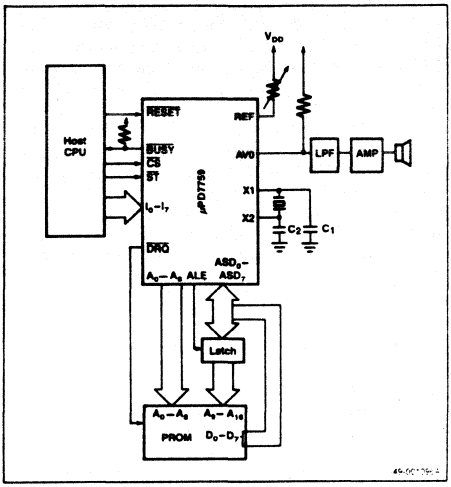
Pin Identification

No.	Symbol	Function
35-39 and 1-3	ASD_0-ASD_7	Higher 8 bits of address output/ speech data input (multiplexed)
4-11	I_0-I_7	Specifies message number; input
12	$\overline{AEN}/\overline{WR}$	Address valid output
13	SAA	Directory data output address valid
14	$\overline{DRQ}$	Data request output signal
15	ALE	High address latch enable output signal
16	REF	Input reference current for DAC
17	AVO	Speech output (analog)
18	$\overline{BUSY}$	Chip busy output
19	$\overline{RESET}$	Initializes device; input
20	GND	Ground
21	$\overline{MD}$	Mode select input (standalone/$\overline{slave}$)
22	$\overline{ST}$	Start synthesis strobe; input
23, 24	X1, X2	Ceramic resonator clock terminals
25	$\overline{CS}$	Chip select input
26-34	A_0-A_8	Lower 9 bits of address output for speech data
40	V_{DD}	Power supply, +5 V (typical)

Sample Circuit: CPU and the μPD7759 Directly Accessed PROM



Sample Application Circuit for the μPD7759



D/A AND A/D CONVERTER

D/A and D/A Converters

Digital-to-Analog

Analog-to-Digital

Sample-and-Hold

Description

The μPC603 is a monolithic digital-to-analog converter designed to convert 6-bit binary coded decimal signals to an analog output voltage signal. The reference voltage, weighted current source, current switch, and output op-amp, are all integrated on board the device.

Features

- ☐ Linearity error: 0.4% (1/4 LSB of 6-bit) max
- ☐ Response speed: 3 μs max
- ☐ Temperature coefficient at full speed: 160 ppm/°C max
- ☐ Input level TTL, DTL level, active low
- ☐ The output voltage range can be applied to any of the 3 following ranges: 0 to 10 V, −5 to +5 V, −10 to +10 V
- ☐ Built-in output short-circuit protection
- ☐ Possesses a linearity equivalent to that of a 7-bit converter, and can be used as a 7-bit D/A converter by the addition of external circuits
- ☐ Pin-for-pin compatible with PMI's "DAC-01C"

Ordering Information

Part Number	Package	Operating Temperature Range
μPC603D	Ceramic DIP	−20°C to +80°C

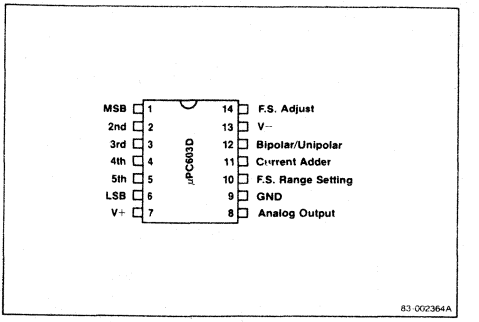
Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V^+ and V^-	±18 V
Power Dissipation	500 mW
Input Voltage	−0.7 to +6 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to +80°C
Storage Temperature Range	−55 to +150°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

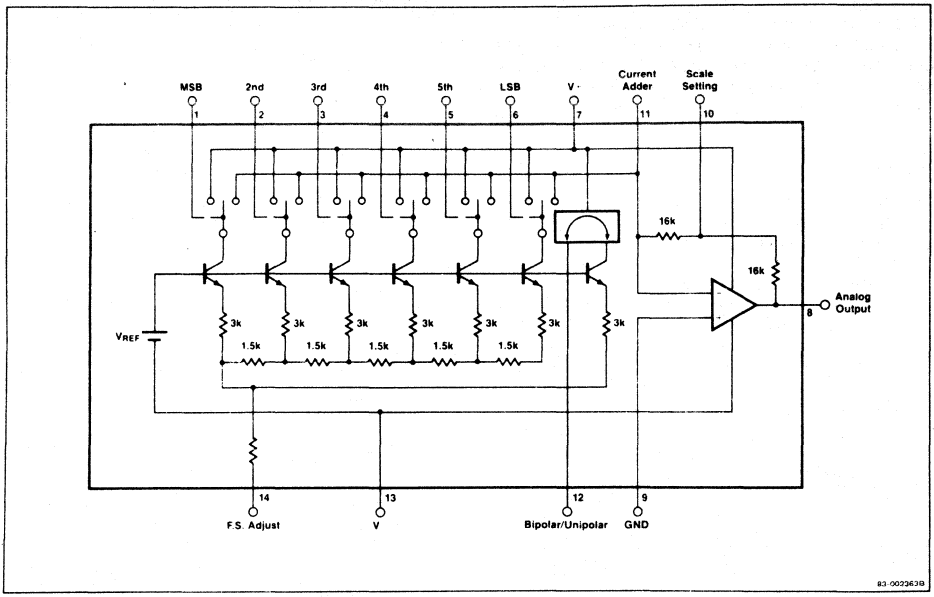
Pin Configuration



Pin Identification

Pin	Name	Function
1	MSB	Data Bit 1
2	2nd	Data Bit 2
3	3rd	Data Bit 3
4	4th	Data Bit 4
5	5th	Data Bit 5
6	LSB	Data Bit 6
7	V+	Power Supply Positive
8	Analog Output	
9	Ground	Power Supply Ground
10	F.S. Range	Full Scale Range Setting
11	Current Adder	
12	Bipolar/Unipolar	Bipolar/Unipolar Control
13	V−	Power Supply Negative
14	F.S. Adj.	Full Scale Adjust

Equivalent Circuit



Electrical Characteristics

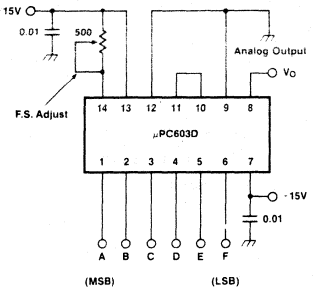
$T_A = +25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Linearity Error	NL			0.4	%FSR	Fig. 1, 2, 3
				0.45	%FSR	Fig. 1, 2, 3; $T_A = -20$ to $+80°C$
Full Scale Temperature Coefficient (Note 2)	$\frac{\Delta I_{FS}}{I_{FS} - \Delta T}$		80	160	ppm/°C FSR	Fig. 1 each bit "ON" after FS adjust $T_A = -20$ to $+80°C$
Analog Output Offset Voltage:						
Unipolar				25	mV	Fig. 1 each bit "OFF" without FS adjust $T_A = -20$ to $+80°C$
Bipolar (Note 3)			50		mV	Fig. 2; ±5 V output without FS adjust
			100		mV	Fig. 3; ±10 V output without FS adjust
Low Level Input Voltage (Note 4)	V_{IL}			0.5	V	Bit "ON"
High Level Input Voltage (Note 4)	V_{IH}	2.1			V	Bit "OFF"
Input Terminal Current	I_{IN}			5.0	μA	$0 V \leq V_{IN} \leq 5 V$
Analog Output FS Voltage:						
Unipolar		+10.00		+11.75	V	$R_L = 2$ kΩ Fig. 1; without FS adjust
Bipolar		+4.93		+5.94	V	Fig. 2: ±5 V range; $R_L = 2$ kΩ without offset adjust and FS adjust
		−5.94		−4.93	V	
		+9.86		+11.89	V	Fig. 3: ±10 V range; $R_L = 2$ kΩ without offset adjust and FS adjust
		−11.89		−9.86	V	
Supply Voltage Rejection Ratio	SVRR			0.15	%FSR/V	$\pm 12 V \leq V^{\pm} \leq \pm 18 V$
Settling Time (Note 5)	T_S			3	μs	Error ≤ ½ LSB, $R_L = 5$ kΩ, $C_L = 30$ pF
Power Consumption	P_D			250	mW	

Notes: 1. %FSR and ppm FSR are the percentage and parts per million against full scale, respectively.
2. The average value of the differential coefficient at $T_C = -20$ to $+80°C$.
3. Care should be taken, since the temperature drift after bipolar offset adjustment has been made will become larger for ICs in which the offset voltage of the bipolar analog output is larger than the LSB value.
4. The input is active "Low."
5. When the load capacitance exceeds 30 pF there is a possibility of oscillation.

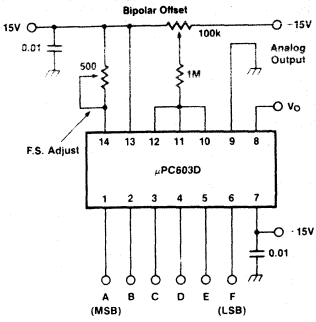
Typical Applications

Unipolar Operation, Output 0 to 10 V Range



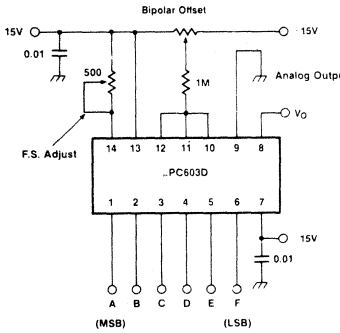
Digital Input	Example		
6 Bit Binary Code	Input		Output
Active Low	111111	=	0.00 V
	100000	≒	4.92 V
	011111	≒	5.08 V
	000000	=	10.00 V

Bipolar Operation (2), −10 V to +10 V Output



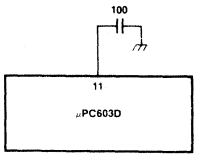
Input 6 Bit Offset	Example		
Binary code	Input		Output
Active Low	111111	=	−10.00 V
	100000	≒	−0.16 V
	011111	≒	+0.16 V
	000000	=	+10.00 V

Bipolar Operation (1), Output −5 V to +5 V Range



Digital Input	Example		
6 Bit Offset	Input		Output
Binary code	111111	≒	−5.00 V
Active Low	100000	≒	−0.08 V
	011111	≒	+0.08 V
	000000	=	+5.00 V

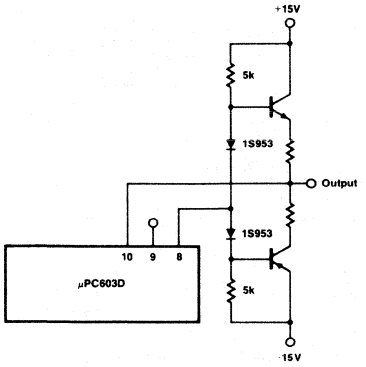
Compensation against Capacitive Loads (1)



- ☐ The IC is stable against capacitive loads of less than 100 pF.
- ☐ Care should be taken, since the settling time will increase to about 5 μs.

Typical Applications (Cont.)

Compensation against Capacitive Loads (2)



- ☐ This method can be applied only to the 0 to 10 V and ±5 V output ranges.
- ☐ It is possible to connect such operational amplifiers as μPC318 etc. to the 8 pin as a voltage follower.

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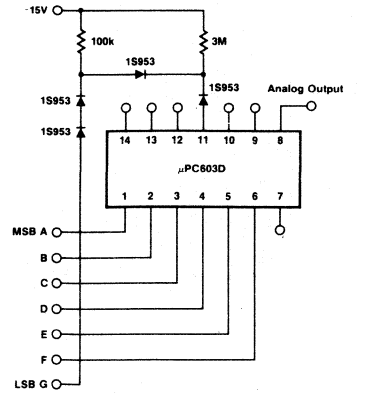
7-Bit D/A Converter



- ☐ The linearity error can be reduced by adjusting the 3 MΩ resistor.
- ☐ The output voltage may be set to any of the 3 ranges, with the circuits of figure 1, 2 and 3.

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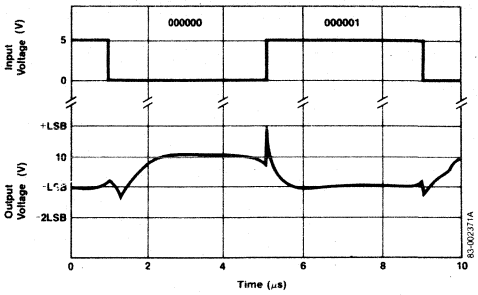
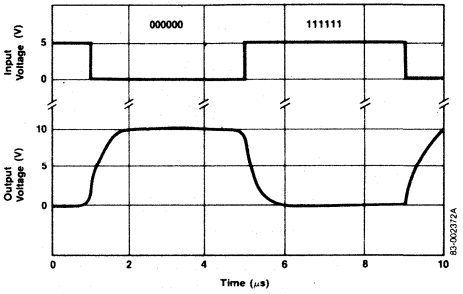
Operating Characteristics

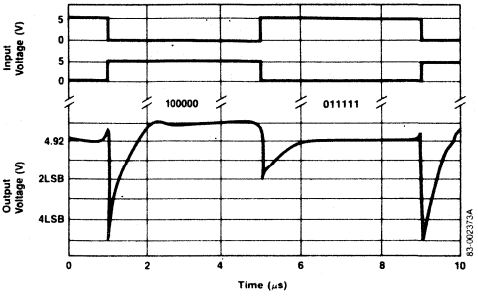
Output Response (1)



Output Response (2)

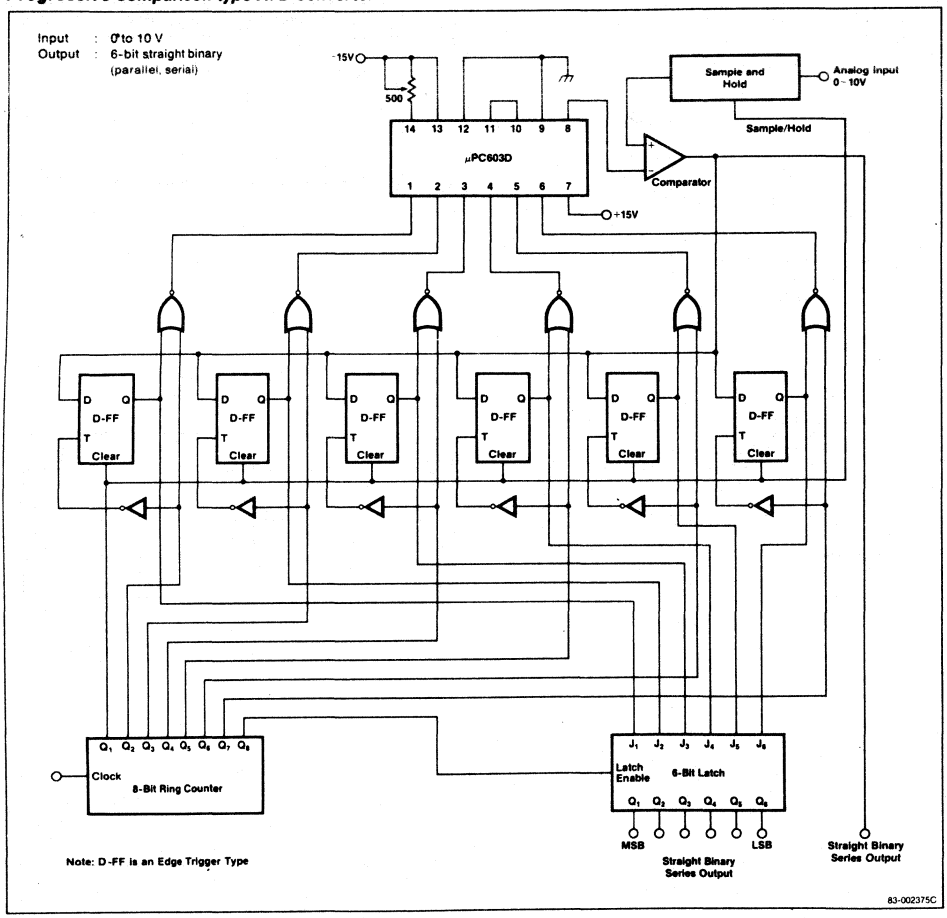


Glitch Waveform at 1/2 Scale



Application Circuits

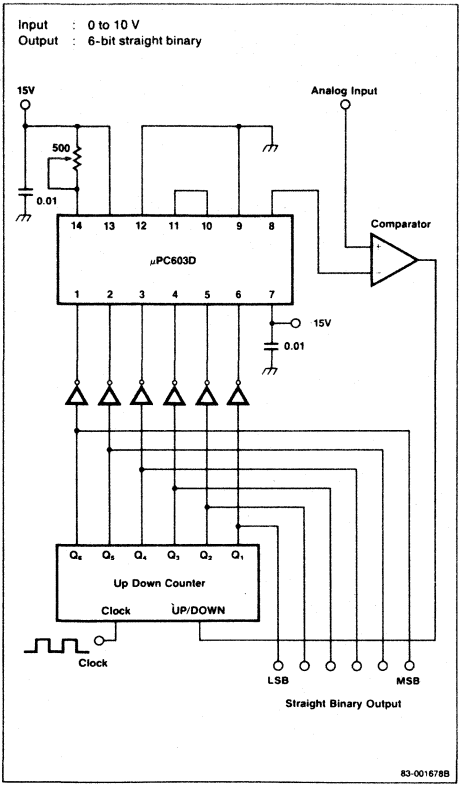
Progressive comparison type A/D converter



Application Circuits (Cont.)

Tracking type A/D converter

Input : 0 to 10 V
Output : 6-bit straight binary



Description

The μPC610 is a high performance precision monolithic digital-to-analog converter which converts 10-bit binary coded digital signals to an analog DC output voltage. All of the necessary circuit blocks are incorporated on board the converter to make designing simple. With the built-in voltage reference and reference input, multiplier operation is also possible.

Features

- ☐ Full Scale Temperature: 100 ppm/°C max
- ☐ Linearity error: 0.2% (1/2 LSB of 8th bit) max
- ☐ Settling Time: 1.5 μs typ
- ☐ Built-in band-gap reference voltage source
- ☐ Multiplying type
- ☐ Sign-Magnitude binary code
- ☐ Low noise
- ☐ Low power dissipation

Ordering Information

Part Number	Package	Operating Temperature Range
μPC610D	Ceramic DIP	−20°C to +80°C

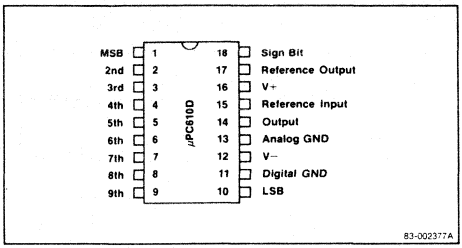
Absolute Maximum Ratings

$T_A = 25°C$

Voltage Between V+ and V−	±18 V
Power Dissipation	500 mW
Analog Ground to Digital Ground	±0.5 V
Logic Input Voltage	−5 to +15 V
Reference Input Voltage	0 to +7 V
Reference Voltage Source Output Current	1.0 mA
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−20 to +80°C
Storage Temperature Range	−55 to +150°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

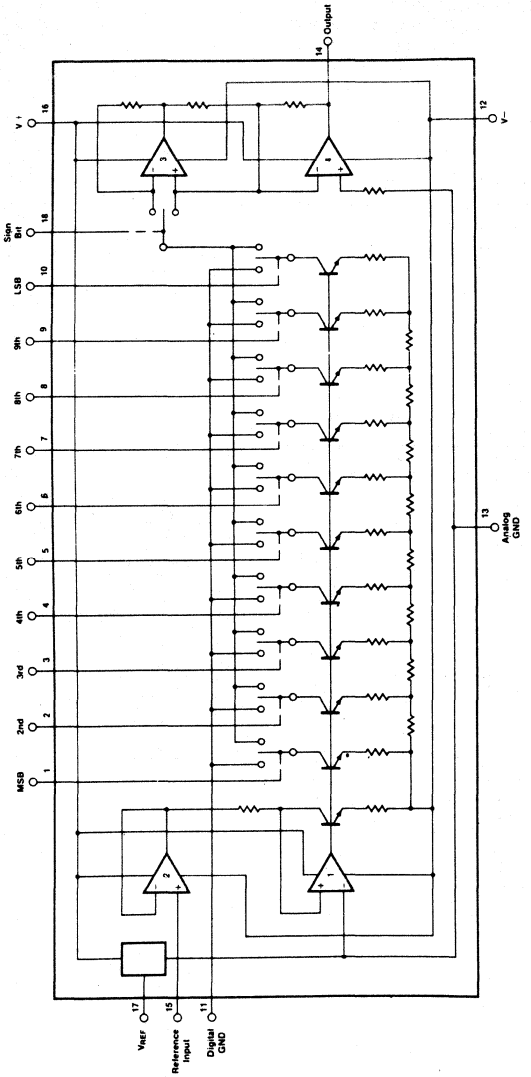
Pin Configuration



Pin Identification

Pin	Name	Function
1	MSB	Data Bit 1
2	2nd	Data Bit 2
3	3rd	Data Bit 3
4	4th	Data Bit 4
5	5th	Data Bit 5
6	6th	Data Bit 6
7	7th	Data Bit 7
8	8th	Data Bit 8
9	9th	Data Bit 9
10	LSB	Data Bit 10
11	Digital Ground	
12	V−, Supply	Power Supply Negative
13	Analog Ground	
14	V_{OUT} − Output	Voltage Output
15	Reference Input	
16	V+ Supply	Power Supply Positive
17	Reference Output	
18	Sign Bit	Sign + or −

Equivalent Circuit



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Electrical Characteristics

$T_A = +25°C$, $V^{\pm} = +15$ V

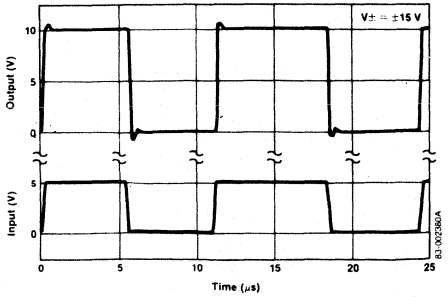
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution (Note 1).				11	Bit	Bipolar Operation
				10	Bit	Unipolar Operation
Linearity Error (Note 1)	NL		0.1	0.2	%FSR	$T_A = -20 \sim +80°C$
Settling Time	T_S		1.5	6.0	μs	Final Value ±20 mV
Full Scale Temperature Coefficient (Note 2)			50	100	ppm/°C	Using internal reference voltage source
			30	60	ppm/°C	Using external reference voltage source
Reference Input Bias Current	I_{IS}		100	500	nA	
Reference Input Slew Rate	SR		1.5		V/μs	
Reference Voltage	V_{REF}	2.2	2.4	2.6	V	$R_L \geq 20$ kΩ
Zero Scale Offset Voltage			±5	±10	mV	Signbit "ON", other bits "OFF"
Zero Scale Offset Symmetry			±1	±5	mV	
Full Scale Output Offset			±10	±80	mV	
Supply Voltage Rejection Ratio	SVRR		0.015	0.15	%FSR/V	$\pm 12\text{ V} \leq V^{\pm} \leq \pm 18\text{ V}$
Power Dissipation	P_D			300	mW	
Logic Input Terminal Current	I_{IN}			10	μA	$V_{IN} = -5\text{ V} \sim +15\text{ V}$
High Level Input Voltage (Note 3)	V_{IH}	2.0			V	
Low Level Input Voltage (Note 3)	V_{IL}			0.8	V	
Full Scale Output Voltage (Note 4)	V_O	10.0		11.0	V	All bits "ON", $R_L \geq 2$ kΩ
		−11.0		−10.0	V	Signbit "OFF", other bits "ON", $R_L \geq 2$ kΩ

Notes: 1. Though the IC possesses a resolution of 10 or 11 bits, the linearity error is equivalent to 9 bits. In applications where perfect monotonicity is expected, employ the IC as an 8-bit D/A converter.
2. The average value of the differential coefficient at $T_A = -20°C$ to $+80°C$.
3. The digital input is active "High" binary code.
4. The value when the internal reference voltage is directly applied to the reference input terminals.

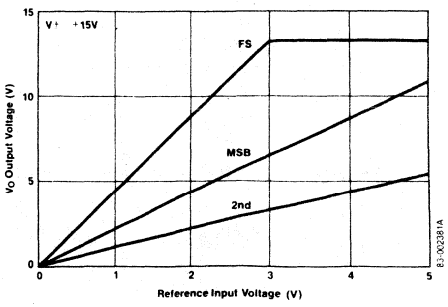
Typical Characteristics

($T_A = 25°C$)

Digital Input Response Characteristics

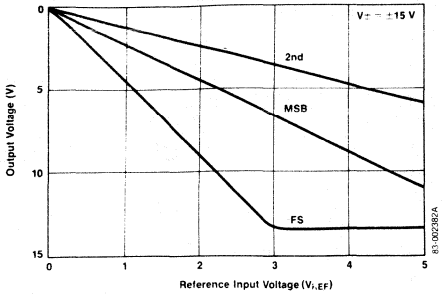


$V_{REF} - V_O$+ Characteristic

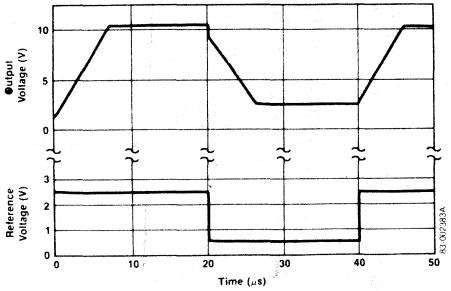


Typical Characteristics (Cont.)
(T_A = 25°C)

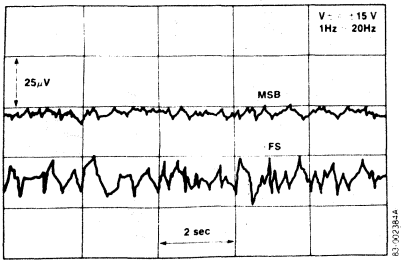
V_{REF} – V_O – Characteristic



Reference Input Response Characteristic

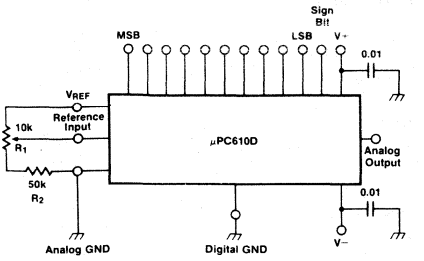


Output Noise Voltage



Typical Applications

Using internal reference voltage source



Note: Use resistors with good stability for R_1 and R_2.

□ Sign + 10-Bit Binary code

Sign	Magnitude	
1	1111111111	=
1	0000000000	= 0 V
0	0000000000	= 0 V
0	1111111111	= 0 V

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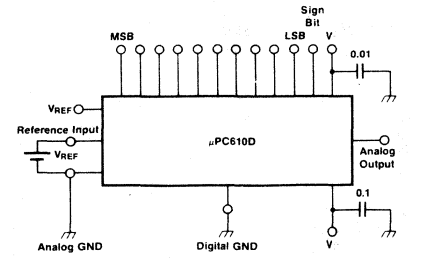
External reference and multiplier type



□ Multiplying coefficient ≈ 4.4
$V_{FS} \approx 4.4 \times V_{REF}$
$V_{MSB} \approx 2.2 \times V_{REF}$
$V_{LSB} \approx 2.2 \times 2^{-9}$

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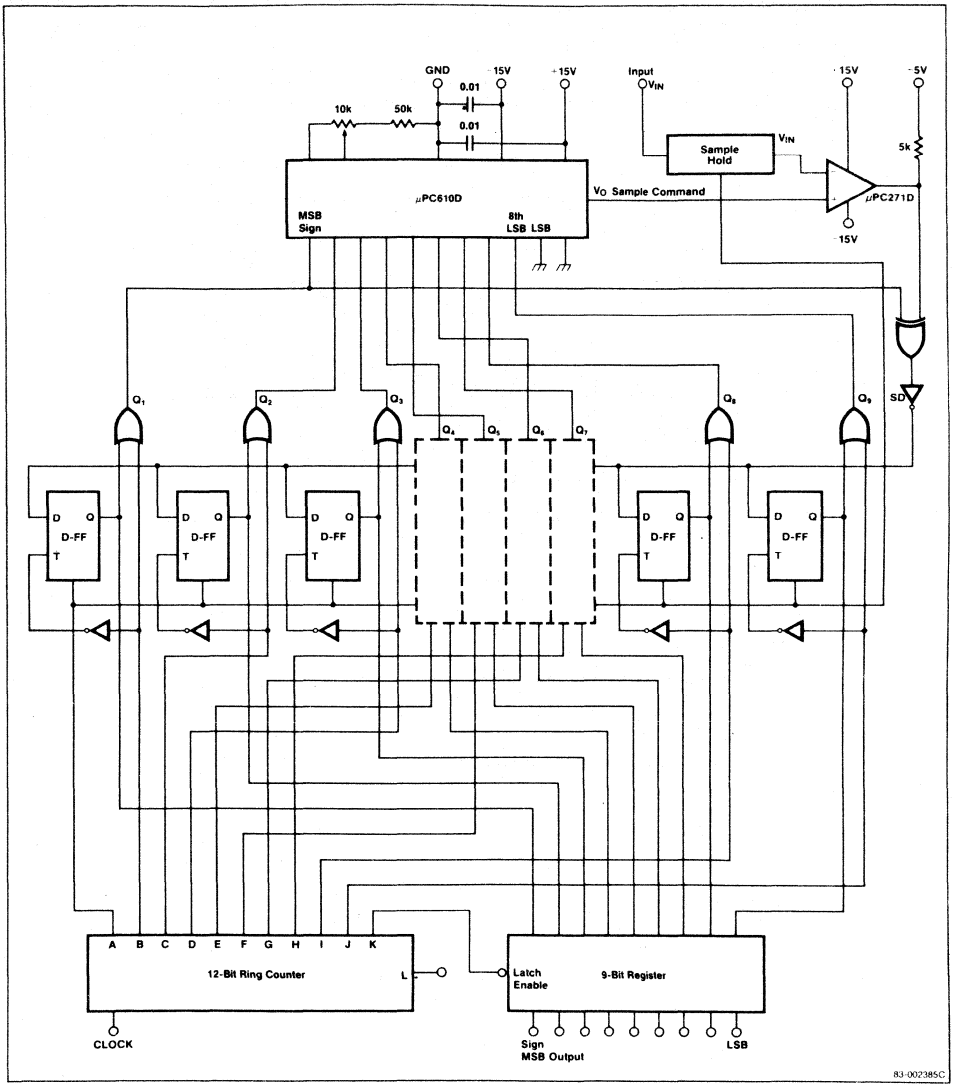
Application Circuits

8-Bit + sign A/D converter

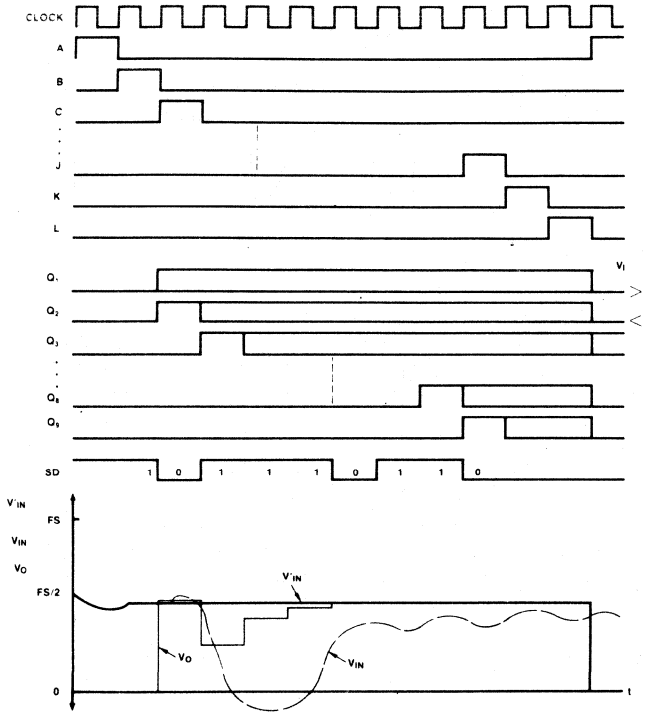
Successive approximation type (sheet 1 of 2)



Application Circuits (Cont.)

8-bit + sign A/D converter

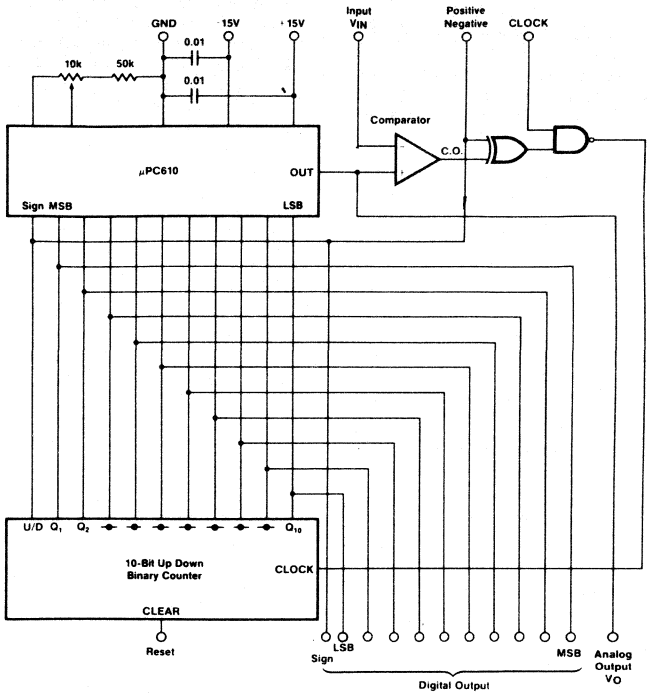
Successive approximation type (sheet 2 of 2)

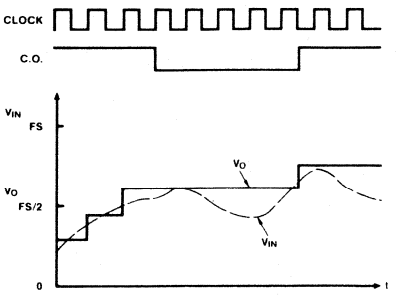


Note: D, V_{IN}, V'_{IN} and V_O show in case when an input equivalent to an output of "101110110".

Application Circuits (Cont.)

Peak detector (positive/negative)





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Precautions for Usage

1. To absorb surges and prevent oscillation, bypass the power supply terminals with a capacitor of 0.01 μF.
2. To utilize the characteristics of the μPC610D in full, employ components of good stability for the full-scale adjustment resistor and the trimmer.
3. Since the settling time may increase or oscillation may occur in the case of capacitive loads, the μPC610D should be used with load capacitance of 100 pF or less.
4. The output amplifier will saturate at: $|V_{REF}| \geq 3$ V in the case of multiplier type operation. In this case the response time and power supply current will increase.
5. Since the reference potential inside the μPC610D is connected to the analog GND, common mode noise in regard to analog GND will present a direct error. Since analog GND and digital GND have independent circuits within the IC, these should be connected together outside the IC (if required).

Description

The μPC624 is a monolithic multiplying digital-to-analog converter designed for high speed performance and design/application flexibility. Advanced circuit design allows settling time of 85 ns. The outputs are high impedance dual complementary current types, which allow simple resistive loading, op-amp voltage conversion, and other configurations. The adjustable threshold logic input allows connection to all popular logic families.

Features

- ☐ Wide range multiplying capability
- ☐ Wide power supply range ±5 V to ±18 V
- ☐ High output impedance and compliance
- ☐ Variable logic threshold
- ☐ Direct interface to TTL, CMOS, PMOS
- ☐ Differential current outputs
- ☐ Pin to pin compatible with PMI'S DAC-08

Ordering Information

Part Number	Package	Operating Temperature Range
μPC624C	Plastic DIP	−20°C to +70°C
μPC624D	Ceramic DIP	−20°C to +80°C

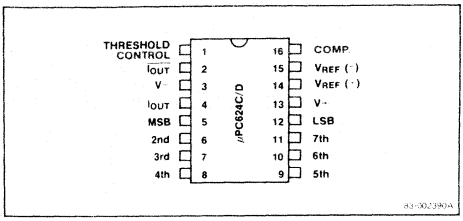
Absolute Maximum Ratings

$T_A = 25°C$

Supply Voltage	36 V
Logic Inputs	V− to (V− +36 V)
Logic Threshold Control Voltage	V− to V+
Analog Current Outputs	4.2 mA
Reference Inputs	V− to V+
Reference Input Differential Voltage	±18 V
Reference Input Current	5.0 mA
Power Dissipation, D or C Package	500 mW
Operating Temperature Range, D Package	−20 to +80°C
Operating Temperature Range, C Package	−20 to +70°C
Storage Temperature Range, D Package	−55 to +150°C
Storage Temperature Range, C Package	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

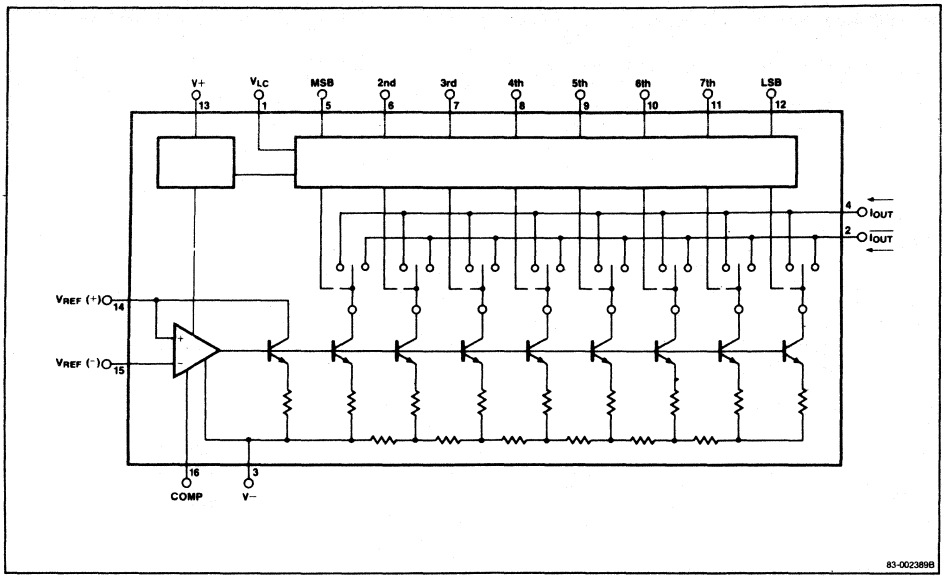
Pin Configuration



Pin Identification

Pin	Name	Function
1	Threshold Control	
2	I_{OUT}	Current Output
3	V−	Power Supply Negative
4	I_{OUT}	Current Output
5	MSB	Data Bit 1
6	2nd	Data Bit 2
7	3rd	Data Bit 3
8	4th	Data Bit 4
9	5th	Data Bit 5
10	6th	Data Bit 6
11	7th	Data Bit 7
12	LSB	Data Bit 8
13	V+	Power Supply Positive
14	$V_{REF}+$	Positive Reference Voltage
15	$V_{REF}-$	Negative Reference Voltage
16	Compensation	Amp Compensation

Equivalent Circuit



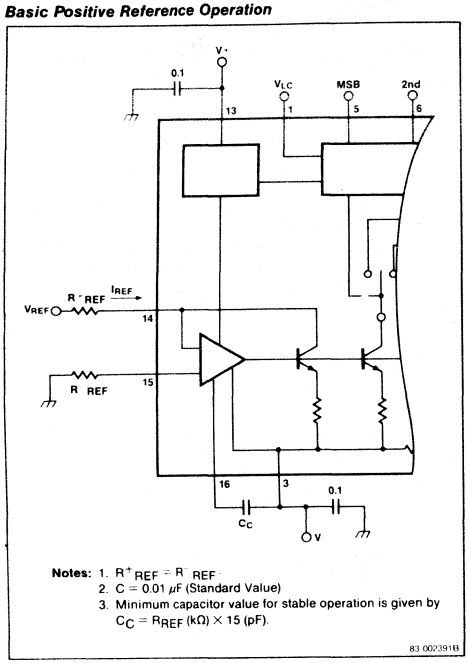
Electrical Characteristics

$T_A = +25°C$, $V^{\pm} = \pm 15$ V, $I_{REF} = 2.0$ mA

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	8	8	Bit	
Monotonicity		8	8	8	Bit	
Nonlinearity	NL			0.19	%FSR	
Settling Time	T_S		85	150	ns	$\pm$½ LSB, $R_L \leq 50\ \Omega$ All bits ON/OFF
Full Scale Temperature Coefficient			10	50	ppm/°C	
Output Voltage Compliance	V_{OC}	−10		+18	V	$\Delta I_{FS} \leq$ ½ LSB
Full Scale Current	I_{FS}	1.94	1.99	2.04	mA	$V_{REF} = 10.000$ V, $R^{+}_{REF} = 5.000$ kΩ
Full Scale Symmetry	$I_{FS} - I_{FS}$		±1.0	±8.0	μA	
Zero Scale Offset Current	I_{ZS}		0.2	2.0	μA	
Output Current Range	I_O	0	2.0	2.1	mA	$V^{-} = 5.0$ V
		0	2.0	4.2	mA	$V^{-} = 8.0$ V to −18 V
Low Level Input Voltage	V_{IL}			0.8	V	$V_{LC} = 0$ V, Bit "OFF"
High Level Input Voltage	V_{IH}	2.0			V	$V_{LC} = 0$ V, Bit "ON"
Low Level Input Current	I_{IL}		−2.0	−10	μA	$V_{LC} = 0$ V, $V_{IN} = -10$ V to +0.8 V
High Level Input Current	I_{IH}		0.002	10	μA	$V_{LC} = 0$ V, $V_{IN} = 2.0$ V to 18 V
Logic Input Swing	V_{IS}	−10		+18	V	
Logic Threshold Range	V_{TH}	−10		+13.5	V	$V_{TH} \approx V_{LC} + 1.3$ V
Reference Bias Current	I_{b+}			−3	μA	
Reference Input Slew Rate	$\Delta I_{REF}/\Delta T$	4.0	8.0		mA/μs	$R_{REF} \leq 200\ \Omega$, $C_C = 0$ pF
Power Supply Voltage Rejection Ratio	SVRR+ V		0.0003	0.01	%FSR/%	$V^{+} = 4.5$ to 18 V, $I_{REF} = 1$ mA
	SVRR− V		0.002	0.01	%FSR/%	$V^{-} = -4.5$ to −18 V, $I_{REF} = 1$ mA
Power Supply Current	I^{+}		2.5	3.8	mA	
	I^{-}		−6.5	−7.8	mA	
	I^{+}		2.4	3.8	mA	$V^{+} = 5$ V, $V^{-} = -15$ V, $I_{REF} = 2$ mA
	I^{-}		−6.4	−7.8	mA	$V^{+} = 5$ V, $V^{-} = -15$ V, $I_{REF} = 2$ mA
	I^{+}		2.3	3.8	mA	$V^{\pm} = \pm 5$ V, $I_{REF} = 1$ mA
	I^{-}		−4.3	−5.8	mA	$V^{\pm} = \pm 5$ V, $I_{REF} = 1$ mA

Typical Applications

Basic Positive Reference Operation



Notes: 1. $R^{+}_{REF} = R^{-}_{REF}$
2. C = 0.01 μF (Standard Value)
3. Minimum capacitor value for stable operation is given by $C_C = R_{REF}$ (kΩ) × 15 (pF).

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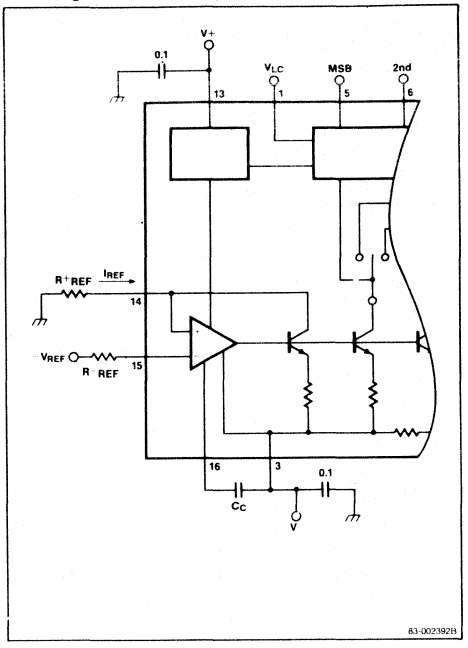
Basic Negative Reference Operation



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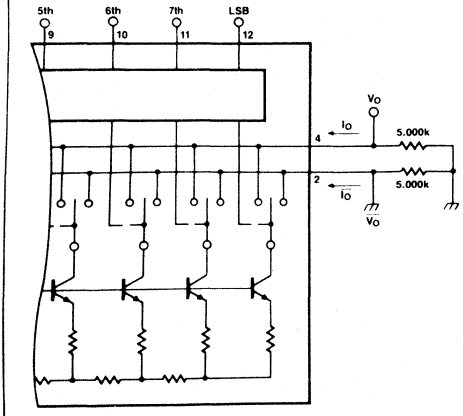
Basic Unipolar Negative Operation



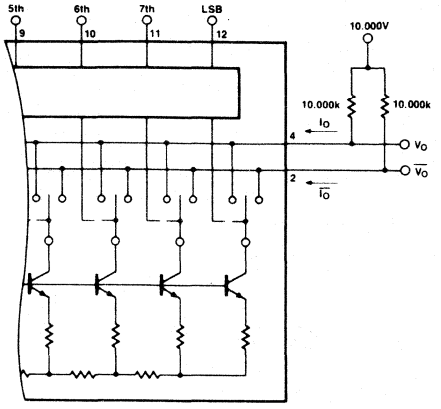
I_{REF} = 2.000 mA

Input	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1	1.992	0.000	−9.96	0.00
1 1 1 1 1 1 1 0	1.984	0.008	−9.92	−0.04
1 0 0 0 0 0 0 1	1.008	0.984	−5.04	−4.92
1 0 0 0 0 0 0 0	1.000	0.992	−5.00	−4.96
0 1 1 1 1 1 1 1	0.992	1.000	−4.96	−5.00
0 0 0 0 0 0 0 1	0.008	1.984	−0.04	−9.92
0 0 0 0 0 0 0 0	0.000	1.992	0.00	−9.96

83-002393B

Typical Applications (Cont.)

Basic Bipolar Output Operation

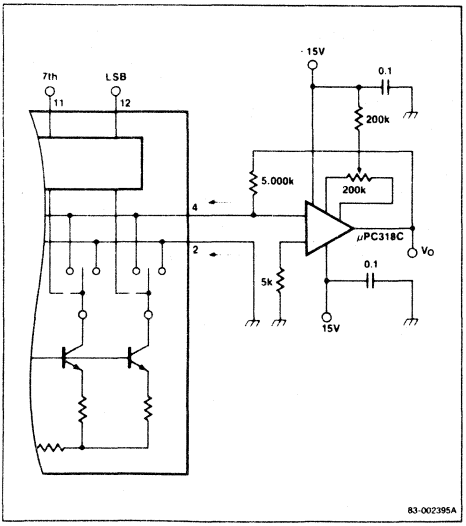


I_{REF} = 2.000 mA

Input	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1	1.992	0.000	−9.92	+10.00
1 1 1 1 1 1 1 0	1.984	0.008	−9.84	+9.92
1 0 0 0 0 0 0 1	1.008	0.984	−0.08	+0.16
1 0 0 0 0 0 0 0	1.000	0.992	0.00	+0.08
0 1 1 1 1 1 1 1	0.992	1.000	+0.08	0.00
0 0 0 0 0 0 0 1	0.008	1.984	+9.92	−9.84
0 0 0 0 0 0 0 0	0.000	1.992	+10.00	−9.92

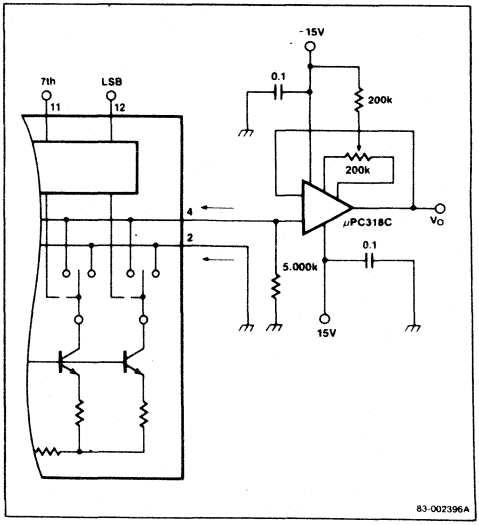
83-002394B

Positive Low Impedance Output Operation



83-002395A

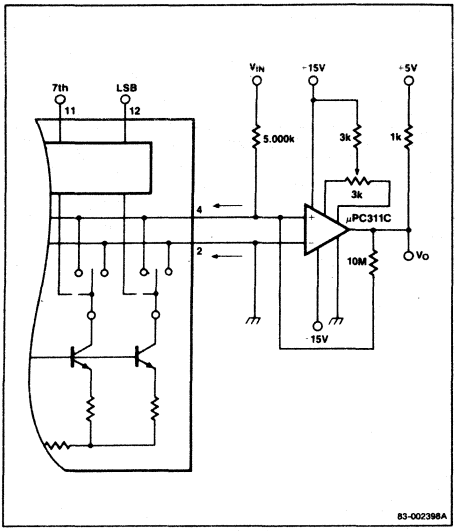
Negative Low Impedance Output Operation



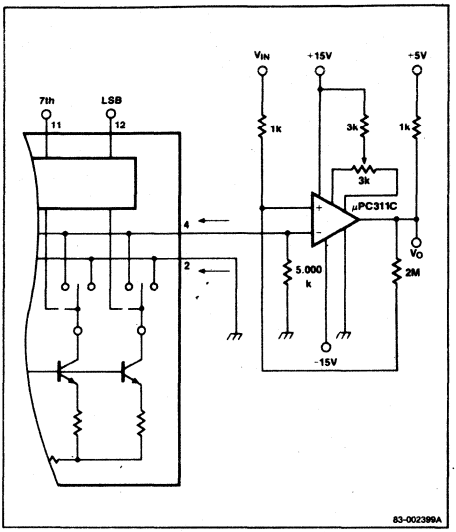
83-002396A

Typical Applications (Cont.)

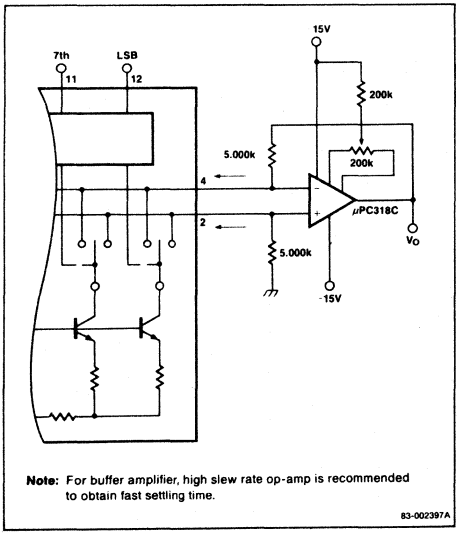
Comparator Connection Method for A/D Conversion
(Positive Analog Input)



Comparator Connection Method for A/D Conversion
(Negative Analog Input)



Low Impedance Output Operation (Both Outputs)



Note: For buffer amplifier, high slew rate op-amp is recommended to obtain fast settling time.

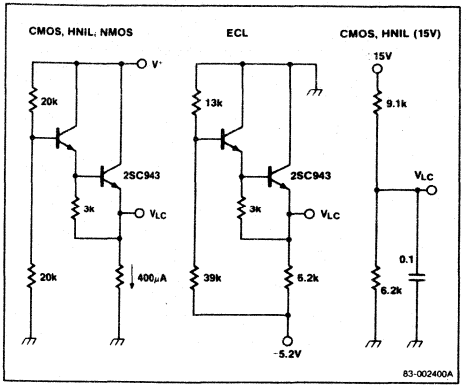
83-002397A

Interfacing with Various Logic Families

The logic threshold is set about 1.4 V above V_{LC}. This enables TTL level acceptance by simply grounding pin 1. By placing an appropriate voltage at the logic threshold control pin (pin 1), various threshold values are available for the other logic families.

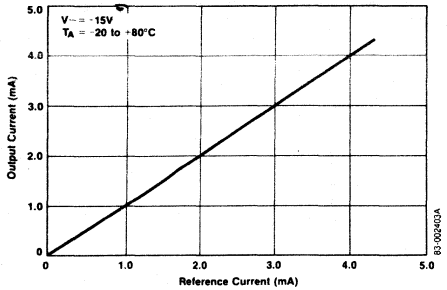
TTL interface permission gives the interval logic threshold −4 mV/°C temperature coefficient. $V_{TH} = V_{LC} + 1.4\ V - 0.004\ V \times (T_A - 25°C)$.

Anti-temperature coefficient circuits

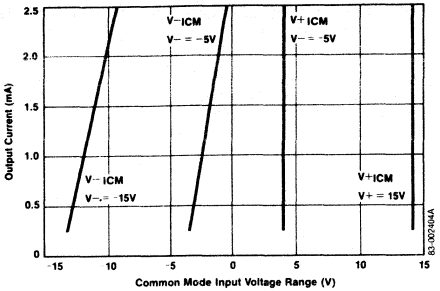


Operating Characteristics
(T_A = 25°C)

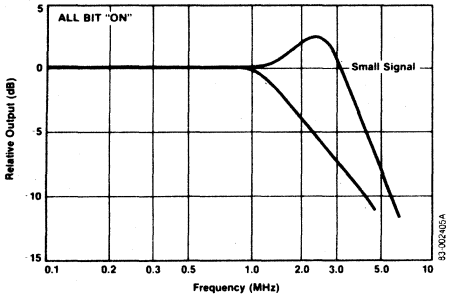
Full Scale Current



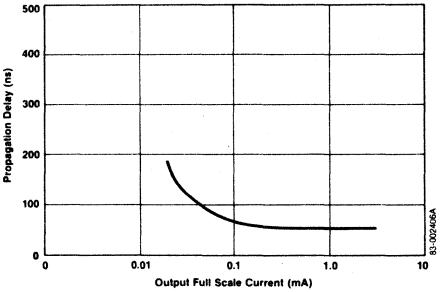
Full Scale Current



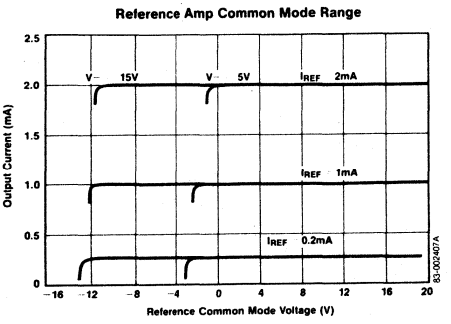
Reference Input Frequency Response



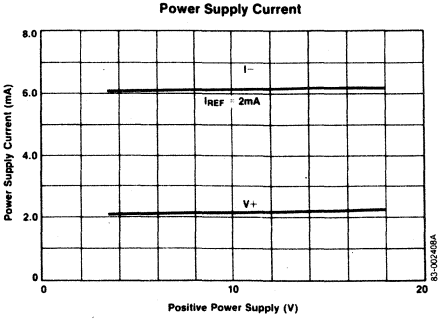
LSB Propagation Delay



Reference Amp Common Mode Range



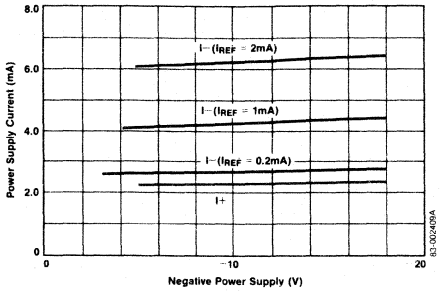
Power Supply Current



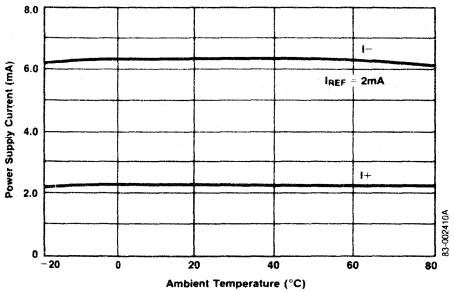
Operating Characteristics (Cont.)

(T_A = 25°C)

Power Supply Current



Power Supply Current



A/D Conversion Program List

0000		MVI	A, 89H	: CONTROL WORD FOR 8255
0002		OUT	(8255)	: PROGRAM TO 8255
0004		MVI	B, 80H	: BIT POINTER INITIALIZE
0006		MOV	A, B	: BIT SET WORD
0007	BIT TEST	OUT	(PORT B)	: BIT SET OUTPUT TO PB OF 8255
0009		MOV	C, A	
000A		NOP		
000B		IN	(PORT C)	: READ COMPARATOR
000D		RRC		: A_0 → CARRY FLG
000E		JC	DEC POINTER	: COMPARATOR TEST
0011		MOV	A, C	
0012		SUB	B	: BIT RESET
0013		MOV	C, A	
0014	DEC POINTER	MOV	A, B	
0015		RRC		: DECREMENT BIT POINTER
0016		JC	RETURN	: LSB WAS TESTED?
0019		MOV	B,A	
001A		ORA	C	: NEW BIT SET WORD
001B		JMP	BIT TEST	
001E	RETURN	RET	(MAIN PROGRAM)	: CONVERSION END & RETURN TO MAIN PROGRAM
	PROGRAM MEMORY		: 31 BYTE	
	CONVERSION TIME		: 371 μs (741 STATE) MAX, 323 μs (645 STATE) MIN (@ ϕ + 2 MHz)	
	WORKING REGISTER		:B & C (C REGISTER; FINAL ANSWER MEMORY)	

Description

The μPC6012 monolithic multiplying digital-to-analog converter is designed to set new standards of speed and accuracy for 12-bit converters. This device is the first 12-bit DAC to use standard processing without the need of thin film resistors and/or active trimming of individual devices. The μPC6012 features high voltage compliance, and high impedance dual complementary outputs, which enable differential operation to effectively double the peak-to-peak output swing. The outputs can be used without op-amps in many applications.

Features

- ☐ Differential nonlinearity to ±0.025% FS max
- ☐ Fast setting time: 400 ns typical
- ☐ Full scale current 4 mA
- ☐ High output impedance and compliance: −5 to +10 V
- ☐ Differential current output
- ☐ High speed multiplying capability
- ☐ Direct interface to TTL, CMOS, ECL, HTL, NMOS
- ☐ Am6012 direct replacement

Ordering Information

Part Number	Package	Operating Temperature Range
μPC6012C	Plastic DIP	0°C to +70°C

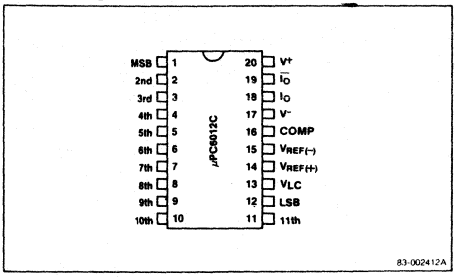
Absolute Maximum Ratings

$T_A = 25°C$

Power Supply Voltage Range, $V^+ - V^-$	36 V
Logic Input Voltage Range, $V^{\pm}$	−5 to +18 V
Output Voltage Range, V_O	−8 to +12 V
Reference Input Voltage Range, V^+_{REF}	V− to V+
Reference Input Differential Voltage Range, $V^+_{REF} - V^-_{REF}$	±18 V
Reference Input Current Range, I_{REF}	0 − 1.25 mA
Total Power Dissipation, P_T	500 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−55 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

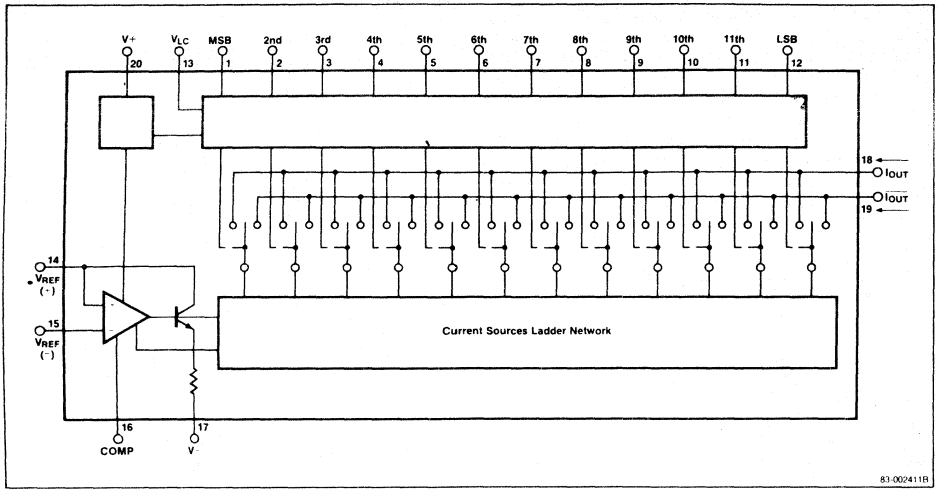
Pin Configuration



Pin Identification Table

Pin	Name	Function
1	MSB	Data Bit 1
2	2nd	Data Bit 2
3	3rd	Data Bit 3
4	4th	Data Bit 4
5	5th	Data Bit 5
6	6th	Data Bit 6
7	7th	Data Bit 7
8	8th	Data Bit 8
9	9th	Data Bit 9
10	10th	Data Bit 10
11	11th	Data Bit 11
12	LSB	Data Bit 12
13	V_{LC}	Threshold Control
14	V_{REF+}	Positive Reference Voltage
15	V_{REF-}	Negative Reference Voltage
16	Compensation	Amp Compensation
17	V− Supply	Negative Supply Voltage
18	I_O	Current Out +
19	$\overline{I_O}$	Current Out −
20	V+ Supply	Positive Supply Voltage

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Voltage	V^+	+4.5	+15		V	
	V^-		−15	−10.8	V	
Ambient Temperature	T_A	0	+25	+70	°C	
Reference Input Current	I_{REF}	0.2	1.0	1.1	mA	
High Level Input Voltage	V_{IH}	+2.0		+18	V	V_{LC} = 0 V
Low Level Input Voltage	V_{IL}	−5.0		+0.8	V	V_{LC} = 0 V
Output Voltage Compliance	V_{OC}	−5.0	0	+10	V	DNL ≤ ±0.025% FSR

Electrical Characteristics

T_A = 0 to 70°C, $V^{\pm}$ = ±15 V, I_{REF} = 1.0000 mA

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Monotonicity		12	12	12	Bit	
Differential Nonlinearity	DNL			±0.025	%FSR	
Nonlinearity	NL			±0.05	%FSR	
Full Scale Output Current	I_{FS}	3.935	3.999	4.063	mA	V_{REF} = 10.000 V, T_A = 25°C, $R_{14} = R_{15}$ = 10.000 kΩ
Full Scale Temperature Coefficient	$\frac{\Delta I_{FS}}{I_{FS} - \Delta T}$			±40	ppm/°C	
Full Scale Symmetry	$I_{FS} - I_{FS}$			±2.0	μA	
Zero Scale Current	I_{ZS}			0.10	μA	
Settling Time	t_s		400		ns	½ LSB, T_A = 25°C, all bits ON or OFF
Propagation Delay	t_{PLH}, t_{PHL}			50	ns	50% to 50%
Output Capacitance	C_O		35		pF	
Logic Input Current	I_{IN}			40	μA	−5 V < V_I < +18 V
Reference Bias Current	I_{b+}			−2.0	μA	
Reference Input Slew Rate	$\lvert\Delta I_{REF}/\Delta t\rvert$	4.0	8.0		mA/μs	C_C = 0, R_{14} = 800 Ω
Supply Voltage Rejection Ratio	$\lvert SVRR^+\rvert$			±0.001	%FSR/%	V+ = +13.5 to +16.5 V, V− = −15 V
	$\lvert SVRR^-\rvert$			±0.001	%FSR/%	V− = +13.5 to −16.5 V, V+ = +15 V
Power Supply Current	I^+1			8.5	mA	V^+ = +5 V
	I^-1			−18.0	mA	V^- = −15 V
	I^+2			8.5	mA	V^+ = +15 V
	I^-2			−18.0	mA	V^- = −15 V
Power Dissipation	P_{D1}			312	mW	V^+ = +5 V, V^- = −15 V
	P_{D2}			397	mW	V^+ = +15 V, V^- = −15 V

Typical Applications

There is a 1 to 4 scale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}).

If $V_{REF} = +10$ V and $I_{FS} = 4$ mA, the value of the R_{REF} is:

$$R^{+}_{REF} = \frac{4 \times 10\ V}{4\ mA}$$

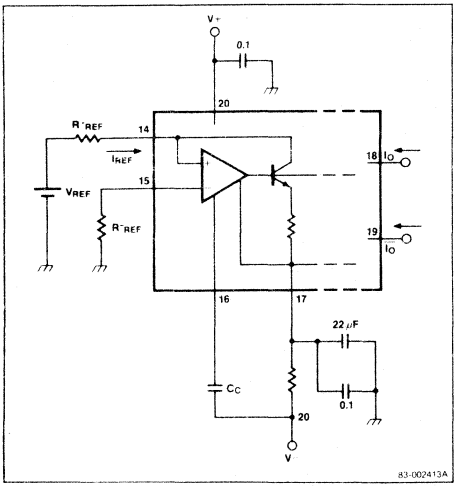
$$R^{+}_{REF} = R^{-}_{REF}$$

The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and is determined by the following expression:

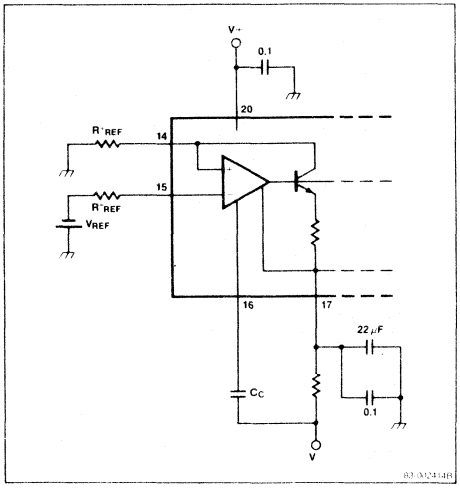
$C = (5\ pF)\ (R+_{REF\ (k\ \Omega)})$.

For $R_{14} < 800\Omega$, no capacitor is necessary.

Positive Reference Voltage

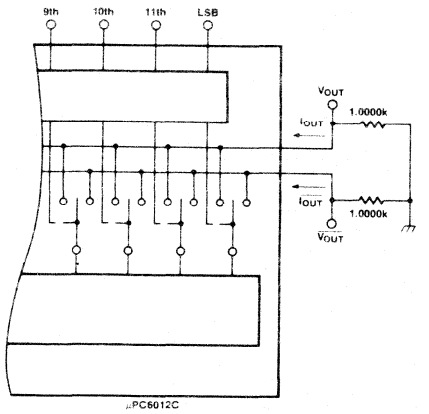


Negative Reference Voltage



Typical Applications (Cont.)

Unipolar Negative Output

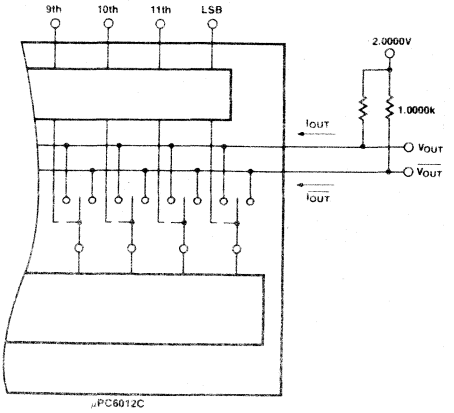


I_{REF} = 1.0000 mA

Input Code MSB ... LSB	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1 1 1 1 1 1 1	3.999	0.000	−3.999	0.000
1 1 1 1 1 1 1 1 1 1 1 1 1 0	3.998	0.001	−3.998	−0.001
1 0 0 0 0 0 0 0 0 0 0 0 0 0	2.000	1.999	−2.000	−1.999
0 0 0 0 0 0 0 0 0 0 0 0 0 1	0.001	3.998	−0.001	−3.998
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000	3.999	0.000	−3.999

83-002415B

Bipolar Output



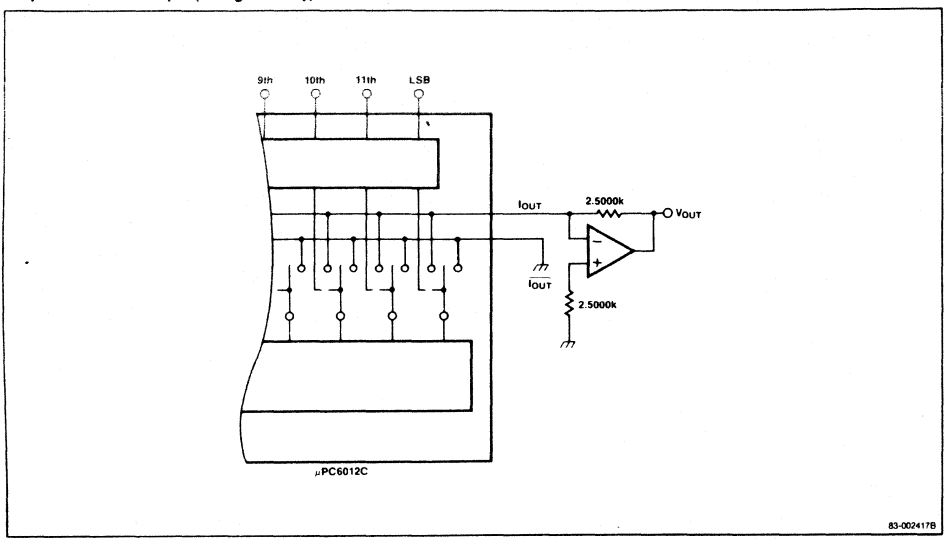
I_{REF} = 1.0000 mA

Input Code MSB ... LSB	I_O (mA)	$\overline{I_O}$ (mA)	V_O (V)	$\overline{V_O}$ (V)
1 1 1 1 1 1 1 1 1 1 1 1 1 1	3.999	0.000	−1.999	+2.000
1 1 1 1 1 1 1 1 1 1 1 1 1 0	3.998	0.001	−1.998	+1.999
1 0 0 0 0 0 0 0 0 0 0 0 0 1	2.001	1.998	−0.001	+0.002
1 0 0 0 0 0 0 0 0 0 0 0 0 0	2.000	1.999	0.000	+0.001
0 1 1 1 1 1 1 1 1 1 1 1 1 1	1.999	2.000	+0.001	0.000
0 0 0 0 0 0 0 0 0 0 0 0 0 1	0.001	3.998	+1.999	−1.998
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000	3.999	+2.000	−1.999

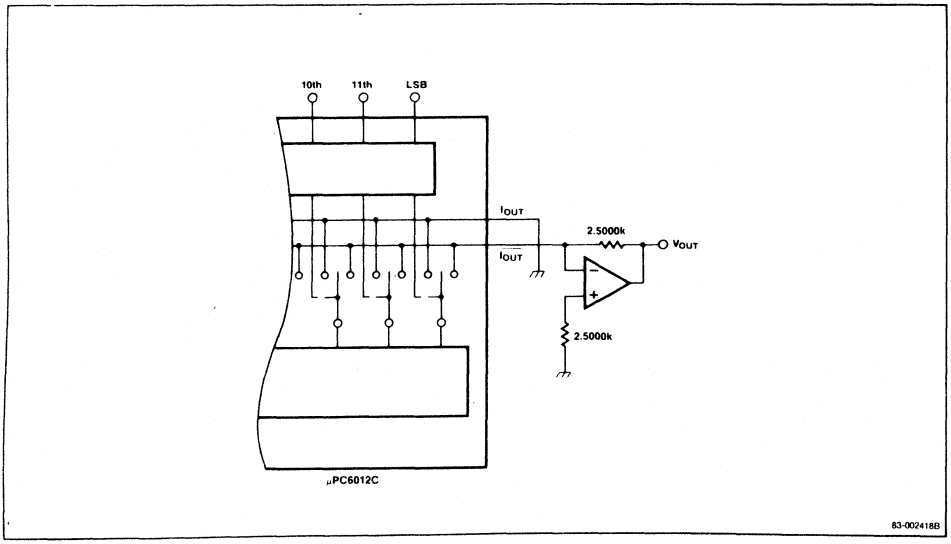
83-002416B

Typical Applications (Cont.)

Unipolar Positive Output (Straight Binary)

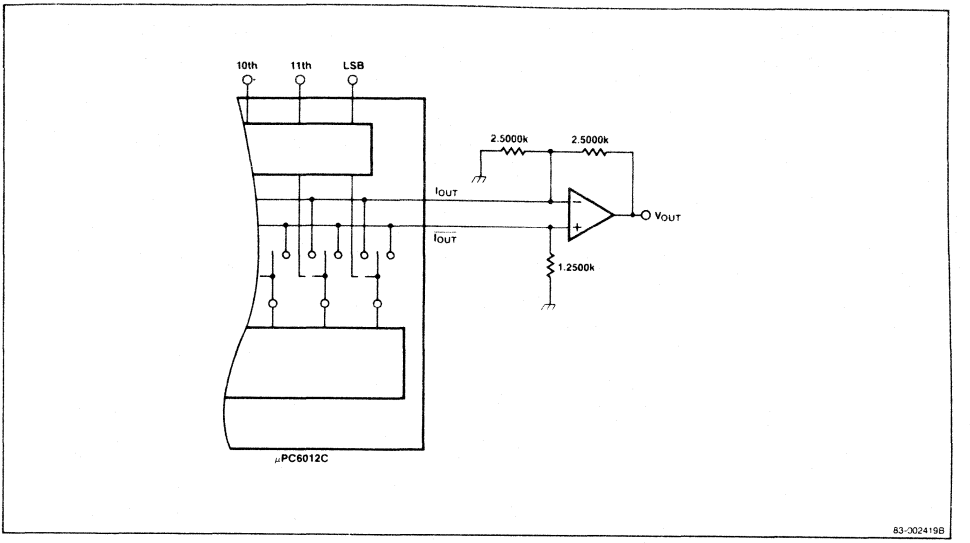


Unipolar Negative Output (Complementary Binary)



Typical Applications (Cont.)

Symmetrical Offset



Description

The μPD6900 is an 8-bit D/A converter for video signals. Although it is a CMOS converter (V+ = 5 V), its conversion rate is very high because a high-speed CMOS processing technique and matrix current cell method are used.

With its low power consumption and conversion rate of 20Msps, this converter can be applied to various units such as digital video processing systems and high-speed facsimiles.

Features

- ☐ Conversion rate: 20 Megasamples/sec
- ☐ Linearity: ±1/2 LSB typ
- ☐ Reference voltage: 2.0 V typ
- ☐ Single 5 V power supply
- ☐ Low power consumption: 150 mW typ.
- ☐ TTL compatible digital input

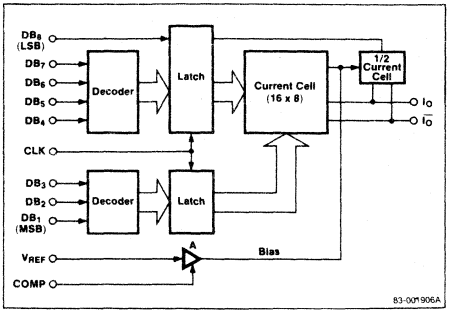
Absolute Maximum Ratings

T_A = 25 °C

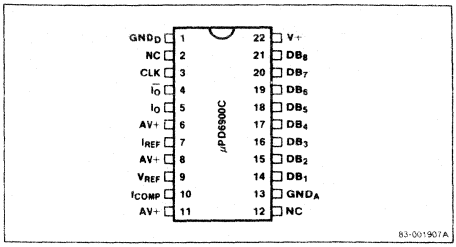
Power supply voltage	−0.3 to +7.0 V
Input/output terminal voltage	−0.3 to V+ +0.3 V
Operating temperature range	−10 to +75 °C
Storage temperature range	−40 to +125 °C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Configuration



Pin Identification

Pin	Symbol	Function
1	GND_D	Digital GND
2	NC	No connection
3	CLK	Clock input
4	$\overline{I_O}$	Complementary current output
5	I_O	Current (analog) output
6	AV+	Analog power supply
7	I_{REF}	Full-scale current adjustment
8	AV+	Analog power supply
9	V_{REF}	Reference voltage input
10	I_{COMP}	Frequency compensation
11	AV+	Analog power supply
12	NC	No connection
13	GND_A	Analog GND
14	DB_1	Digital input (MSB)
15	DB_2	Digital input (2nd)
16	DB_3	Digital input (3rd)
17	DB_4	Digital input (4th)
18	DB_5	Digital input (5th)
19	DB_6	Digital input (6th)
20	DB_7	Digital input (7th)
21	DB_8	Digital input (LSB)
22	V+	Digital power supply

Ordering Information

Part Number	Package	Operating Temperature Range
μPD6900C	Plastic DIP	−20 °C to +75 °C

Pin Function

DB_1 to DB_8

DB_1 to DB_8 are the 8-bit digital signal input terminals. DB_1 corresponds to MSB, and DB_8 corresponds to LSB.

CLK

CLK is the sampling clock input terminal. An 8-bit digital signal is latched within the IC by the rising edge of the sampling clock and is converted into an analog signal.

I_O

I_O is the analog output terminal. This output is current output. It outputs the current of 10 mA (typ) at the full scale (Reference voltage = 2 V, R_{REF} = 800 Ω).

$\overline{I_O}$

$\overline{I_O}$ is the complementary current output terminal.

I_{REF}

I_{REF} is the full-scale current adjustment terminal. Normally, a resistance of 800 Ω is set between this terminal and GND_A. (When V_{REF} is 2.0 V, the full-scale current I_{FS} is 10 mA typ.)

V_{REF}

V_{REF} is the reference voltage input terminal. Normally, the input level is 2.0 V.

f_{COMP}

f_{COMP} is the terminal to which a frequency compensation capacitor should be connected. Normally, a capacitance of 1.0 μF is set between this terminal and GND_A.

AV+

AV+ is the power supply terminal (+5 V) for an analog system.

GND_A

GND_A is the ground terminal for an analog system.

V+

V+ is the power supply terminal (+5 V) for a digital system.

GND_D

GND_D is the ground terminal for a digital system.

NC

NC is a non-connection terminal, but normally it is connected to GND_A.

Recommended Operating Conditions

T_A = −20 to +75 °C

Parameter	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage	V+, AV+	4.5	5.0	5.5	V	
Reference voltage	V_{REF}	1.8	2.0	2.2	V	
Reference resistance	R_{REF}		800		Ω	
Sampling clock	f_{SAMP}	DC		20	MHz	
Sampling clock low level pulse width	t_{PWL}	10			ns	
Sampling clock high level pulse width	t_{PWH}	10			ns	
Data set up time	t_S	20			ns	
Data hold time	t_H	10			ns	
Digital input high level	V_{IH}	2.7			V	
Digital input low level	V_{IL}			0.4	V	
Compensation capacitance	C_{COMP}	1.0			μF	

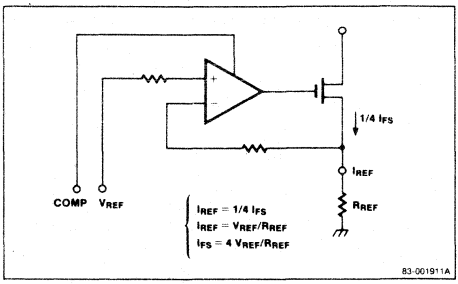
Electrical Characteristics

T_A = −20 to +75 °C, V+ = AV+ = 5 V ± 10%

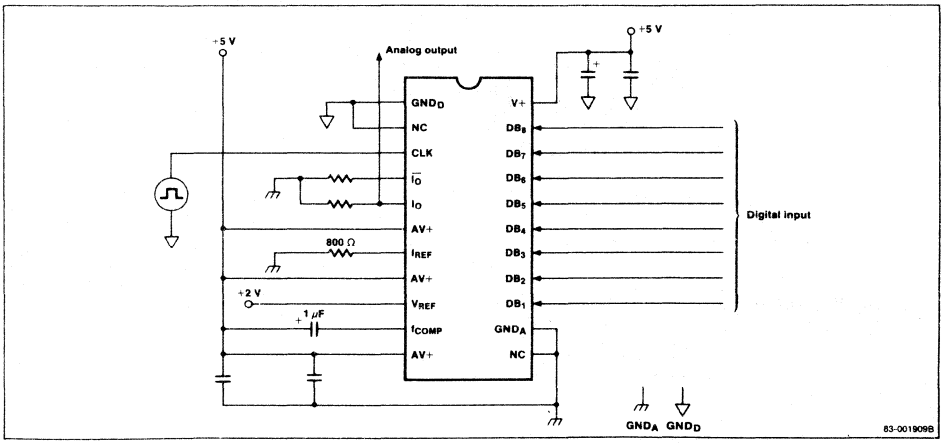
Parameter	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Power supply current	I+		30	50	mA	
Resolution			8		bit	
Non-linearity error	NL		±1/2	±1	LSB	
Differential non-linearity	DNL		±1/2	±1	LSB	
Differential gain	DG		3	4	%	f_{SAMP} = 14.318 MHz
Differential phase	DP		1	3	°	f_{SAMP} = 14.318 MHz
Output compliance	V_O	2.5	3.0		V	V+ = 5.0 V
Analog output delay time	t_d		40		ns	
Settling time	t_{SET}		40		ns	
Full-scale current	I_{FS}	9	10	11	mA	
Zero-scale offset current	I_{ZS}			20	μA	
Digital input capacitance	C_{IN}			30	pF	
Digital input current	I_{IN}			10	μA	

Typical Applications

Full-Scale Current (I_{FS}) Setting Method

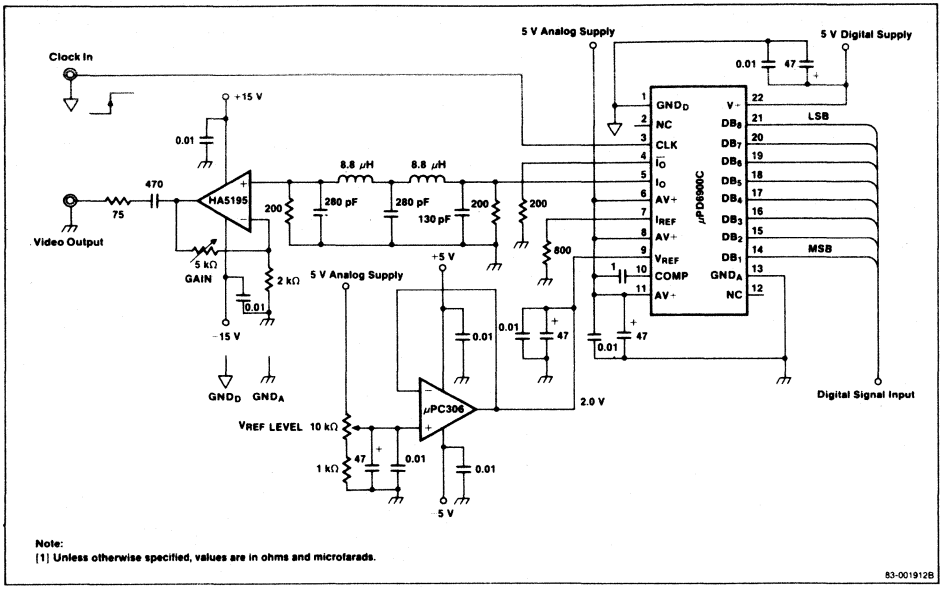


Test Circuit

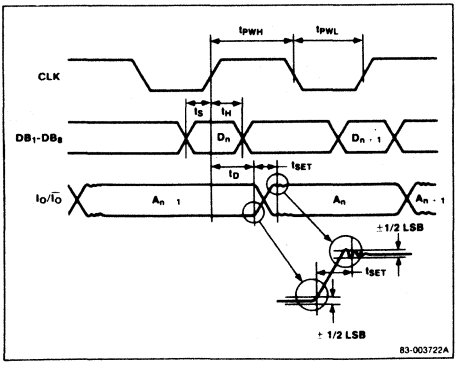


Typical Applications (Cont.)

Application Circuit



Timing Waveforms



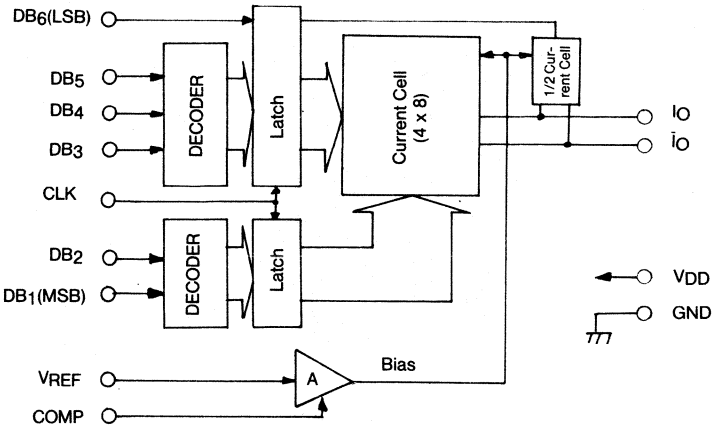
6-bit D/A converter CMOS

The μPD6901C is an 6-bit D/A converter for video signals.
Although it is a CMOS converter (V_{DD} = 5V), its conversion rate is very high because a high speed CMOS processing technique and a matrix current cell method are used.
With its low power comsumption and conversion rate of 20Msps, this converter can be applied to various units such as digital Video processing systems and high-speed facsimiles.

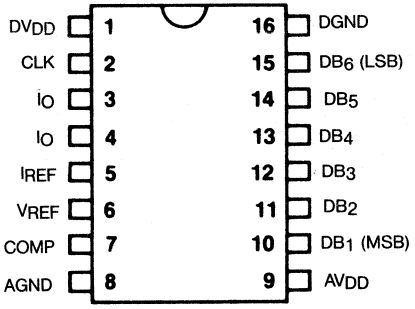
Features

- 6-bit D/A converter
- Conversion rate: 20Msps
- Liniarity: ±1/2 LSB
- Reference voltage: 2.0 V typ.
- Power supply voltage: +5V single
- Low power comsumption (110mW typ.)
- TTL compatible (Digital input)
- 16 pin plastic DIP

Block Diagram



Connection Diagram (Top View)



1	DV_{DD}	Digital power supply
2	CLK	Clock input
3	$\bar{I}_O$	Complementary current output
4	I_O	Current output
5	I_{REF}	Full-scale current adjustement
6	V_{REF}	Reference voltage input
7	COMP	Amp compensation
8	AGND	Analog GND
9	AV_{DD}	Analog power supply
10	DB_1	Digital input (MSB)
11	DB_2	Digital input (2nd)
12	DB_3	Digital input (3rd)
13	DB_4	Digital input (4th)
14	DB_5	Digital input (5th)
15	DB_6	Digital input (LSB)
16	DV_{DD}	Digital power supply

Pin Discription

Symbol	Function
DB_1–DB_6	DB_1 to DB_6 are the 6-bit digital signal input terminals. DB_1 corresponds to MSB, and DB_6 corresponds to LSB.
CLK	CLK is the sampling clock input terminal. An 6-bit digital signal are latched within the IC by the rising edge of the sampling clock and are converted into an analog output signal.
I_O	I_O is the analog output terminal. This output is current output. It outputs the current of 10mA at the full-scale.
$\overline{I_O}$	$\overline{I_O}$ is the complementary current output terminal.
I_{REF}	I_{REF} is the full-scale current adjustement terminal. Normally, a resistance of 800 ohms is set between this terminal and AGND. (When V_{REF} is 2.0V, the full-scale current I_{FS} is 10mA typ.)
V_{REF}	V_{RREF} is the reference voltage input terminal. Normally, the input level is 2.0V.
COMP	COMP is the terminal to which amp compensation condenser should be connected. Normally, the a capacitance of 1.0μF is set between this terminal and AGND.
AV_{DD}	AV_{DD} is the power supply terminal (+5V) for an analog system.
AGND	AGND is the ground terminal for an analog system.
DV_{DD}	DV_{DD} is the power supply terminal (+5V) for a digital system.
DGND	DGND is the ground terminal for a digital system.

Absolute Maximum Ratings (T_a = 25°C)

Paramater	Rating	Unit
Power supply voltage	−0.3 to +7.0	V
Input terminal voltage	−0.3 to V_{DD}+0.3	V
Output terminal voltage	−0.3 to V_{DD}+0.3	V
Operating temperature range	−10 to +75	°C
Strage temperature range	−40 to +125	°C

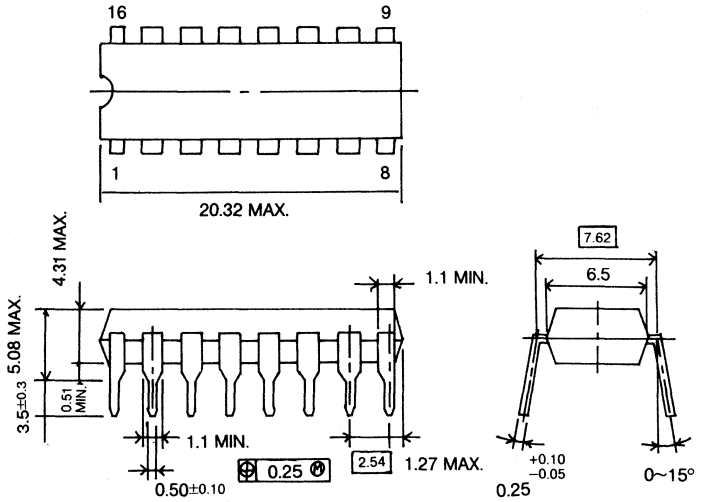
Recommended Operating Condition (T_a = 25°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply vol ge	V_{DD}		4.5	5.0	5.5	V
Reference voltage	V_{REF}			2.0		V
Reference resistance	R_{REF}			390		Ω
Sampling clock	f_{samp}		DC		20	MHz
Digital input high level	V_{IH}		2.7			V
Digital input low level	V_{IL}				0.4	V
Compensation capacity	C_{COMP}		1.0			μF

Electrical Characteristiscs (T_a = 25°C, V_{DD} = 5V, f_{samp} = 20MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD}			22		mA
Resolution	RES			6		bit
Non-linearity error	NL				±1/2	LSB
Differencial non-linearity	DNL				±1/2	LSB
Differencial gain	DG			2		%
Differencial phase	DP			2		°
Output compliance	V_O	V_{DD} = 5.0V	2.5			V
Full-scale current	I_{FS}			10		mA

Package Dimensions (Unit : mm)
16 pin plastic DIP (300 mil)



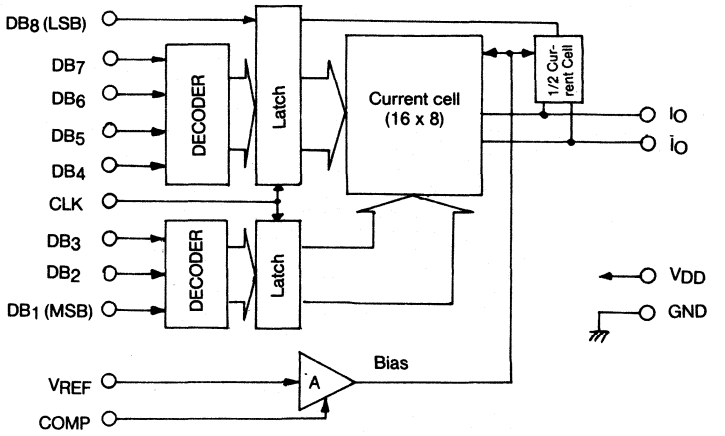
8-bit 50Msps D/A Converter CMOS

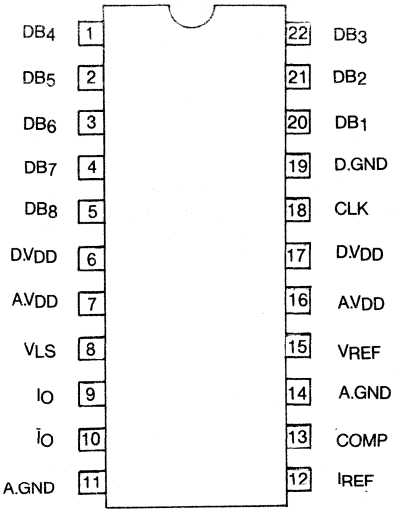
The μPD6902C is an 8-bit D/A converter for use in video applications. The high-speed CMOS processing technology and the matrix current cell method adapted for this CMOS device have fast conversion rates to be achieved. Conversion rates of up to 50 Msps can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and video systems.

Features

- Resolution: 8 bits
- Conversion rate: 50 Msps
- Liniarity: ±1/2 LSB TYP.
- Reference voltage: 2.5 V TYP.
- Power supply voltage: +5V single
- Low power comsumption (400mW TYP.)
- TTL compatible (Digital inputs)
- 22 pin plastic DIP

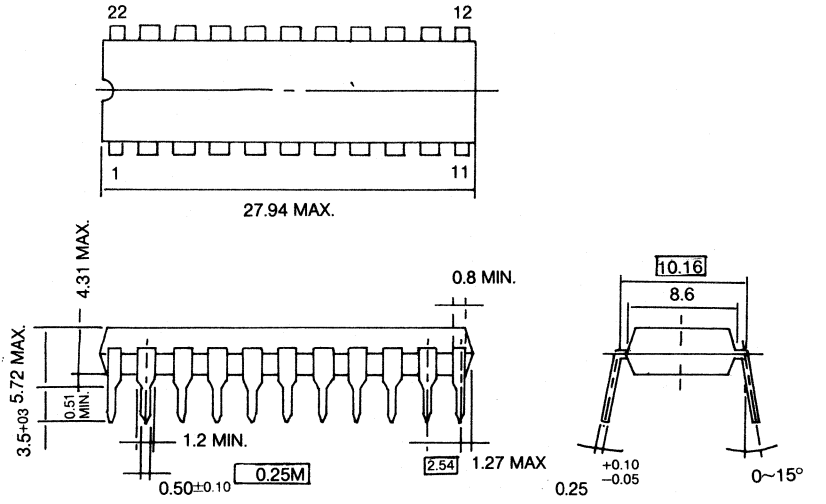
Block Diagram





1	DB_4	Digital input (4th)
2	DB_5	Digital input (5th)
3	DB_6	Digital input (6th)
4	DB_7	Digital input (7th)
5	DB_8	Digital input (LSB)
6	DV_{DD}	Digital power supply
7	AV_{DD}	Analog power supply
8	V_{LS}	Digital input level select (TTL/CMOS)
9	I_O	Current output
10	$\bar{I}_O$	Complementary current output
11	AGND	Analog GND
12	I_{REF}	Full-scale current adjustment
13	COMP	Amp compensation
14	AGND	Analog GND
15	V_{REF}	Reference voltage input
16	AV_{DD}	Analog power supply
17	DV_{DD}	Digital power supply
18	CLK	Sampling clock input
19	DGND	Digital GND
20	DB_1	Digital input (MSB)
21	DB_2	Digital input (2nd)
22	DB_3	Digital input (3rd)

Package Dimensions (unit; mm)
22-pin plastic DIP (400 mil)



P22C-100-400B

Description

The μPD7011 is a low cost 8-bit NMOS digital-to-analog converter featuring single +5 V power supply operation and on-board voltage reference. The serial interface option allows easy interface to the μCOM-43, -87, and -75 series of single chip microcomputers and the μPD7720 Signal Processing chip (SPI). In parallel mode the μPD7011 is easily connected to the 8080 and 8085 type bus structures by the bus interface facilities.

Features

- ☐ Single +5 V power supply
- ☐ Internal voltage reference
- ☐ Complementary current output
- ☐ Wide output compliance (2.4 V to 8 V)
- ☐ Serial interface with μCOM-43, -87, -75 and μPD7720 (SPI)
- ☐ Bus interface with 8080 and 8085A-2
- ☐ Pure binary and 2's complement code available in serial mode
- ☐ MSB 1st and LSB 1st serial input available
- ☐ Applications: CPU peripherals, toys, displays, instrumentation, speech synthesis
- ☐ Two performance ranges linearity error: μPD7011C, 1 LSB; μPD7011C-1, 1/2 LSB

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7011C	Plastic DIP	−20°C to +70°C

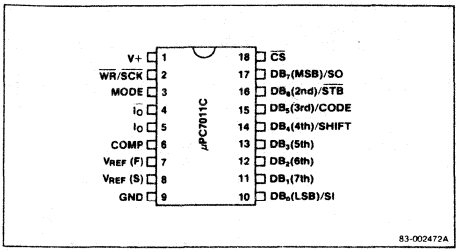
Absolute Maximum Ratings

$T_A = 25°C$

Operating Temperature	−20°C to +70°C
Storage Temperature	−65°C to +125°C
All Input Voltages	−0.3 to V_{DD} + 0.3 V
Power Supply	−0.3 V to +7.0 V
Power Dissipation	300 mW
SO Pin Pull-up Voltage	V_{DD} + 0.3 V
$I_O/\overline{I_O}$ Output Pull-up Voltage	+10 V

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

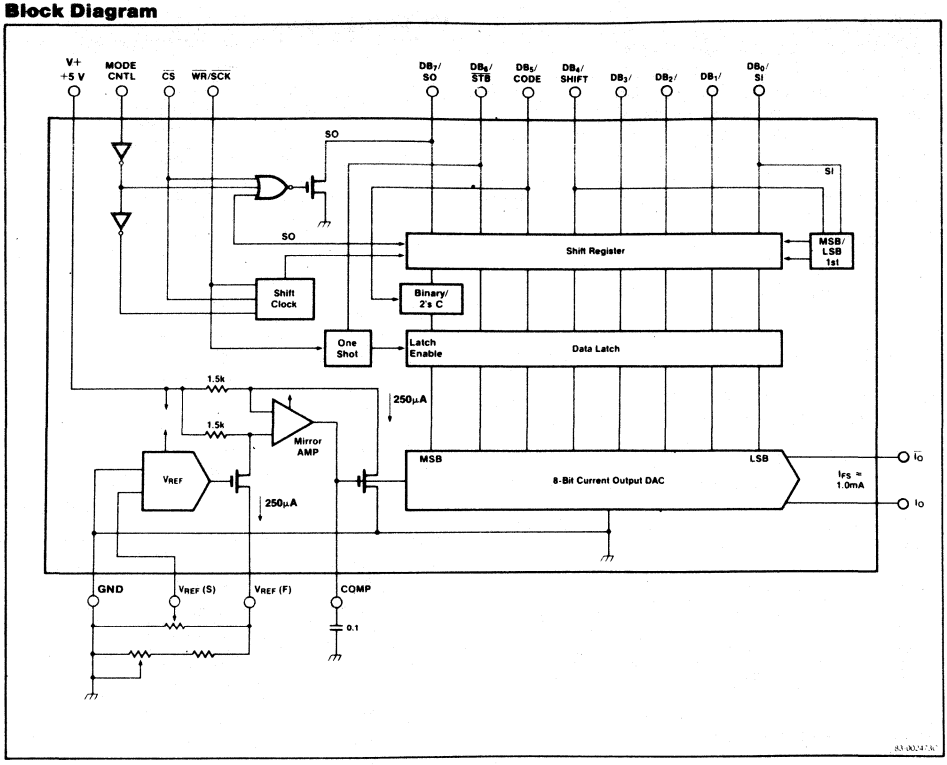
Pin Configuration



Pin Identification

Pin	Name	Function
1	V+	+5 V power supply
2	WR/SCK	WR: write SCK: serial shift clock
3	MODE	High: serial input mode Low: parallel bus input mode
4	$\overline{I_O}$	Complementary current outputs (open drain)
5	I_O	
6	COMP	Frequency compensation
7	V_{REF}(F)	Voltage reference output
8	V_{REF}(S)	Reference sense
9	GND	Digital analog common GND
10	DB_0/SI	Serial data input (serial) LSB input (bus)
11	DB_1	7th bit input (bus)
12	DB_2	6th bit input (bus)
13	DB_3	5th bit input (bus)
14	DB_4/SHIFT	Shift select: High: MSB 1st Low: LSB 1st 4th bit input (bus)
15	DB_5/CODE	High: 2s complement code Low: pure binary code 3rd bit input (bus)
16	$DB_6/\overline{STB}$	Strobe input 2nd bit input (bus)
17	DB_7/SO	Serial output (open drain) MSB input (bus)
18	$\overline{CS}$	Chip select

Block Diagram



DC Characteristics

$T_A = 25°C \pm 2°C$; $I_{FS} = 1$ mA;
$C_{COMP} = 0.1\ \mu F$; $V+ = 5\ V \pm 5\%$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	8	8	Bits	−20°C to +70°C
Nonlinearity, 7011C-1	NL		0.25	0.5	LSB	−20°C to +70°C
Nonlinearity, 7011C	NL		0.5	1	LSB	−20°C to +70°C
Differential Nonlinearity	DNL		0.1	0.1	LSB	−20°C to +70°C
Zero-Scale Error				0.5	LSB	−20°C to +70°C
Zero-Scale Symmetry		−1.5	−1.0	0.5	LSB	Note 1
Gain Error, 7011C-1				3	%FSR	Note 2
Gain Error, 7011C				5	%FSR	Note 2
Full-Scale Symmetry		−1.5	−1.0	−0.5	LSB	Note 3
Reference Voltage	V_{REF}	1.41	2.0	2.59	V	
Power Supply Current	I_{DD}		8	13	mA	
Logic Input Leakage	I_{ILK}		0.1	10	μA	$0 \le V_{IN} \le V+$
Low-Level Output Voltage	V_{OL}			0.5	V	SO (Pin 17) $I_{SINK} \le 2$ mA
Output Leakage	I_{OH}		0.1	10	μA	SO (pin 17) $V_O = V+$
Full-Scale Drift			70		PPM/°C	$\Delta I_{FS}/\Delta T$
Supply Voltage 7011C-1 Rejection Ratio	SVRR			0.8	%FSR/V	$\Delta I_{FS}/\Delta T$
Supply Voltage 7011C Rejection Ratio	SVRR			1.2	%FSR/V	$\Delta I_{FS}/\Delta V^+$
Analog Output Compliance		2.4		8.0	V	$\Delta I_{O(FS)} \le$ 1 LSB

Notes: 1. Zero-scale symmetry is defined as follows: $255(I_O(ZS) - \overline{I_O}(ZS)/I_O(FS)$.
2. Gain error is defined as follows: $100(I_O(FS) \times 256/255 - 4I_{REF})/4I_{REF}$.
3. Full-scale symmetry is defined as follows: $255(I_O(ZS) - \overline{I_O}(ZS))/I_O(FS)$.

Recommended Operating Conditions

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit
Supply Voltage	$V+$	4.75	5.0	5.25	V
Reference Current	I_{REF}	225	250	275	μA
Full-Scale Current	I_{FS}	0.9	1.0	1.1	mA
Reference Force Terminal Voltage	V_{REF}	2.65	2.7	2.75	V
Low-Level Logic Input	V_{IL}	0		0.8	V
High-Level Logic Input	V_{IH}	2.0		$V+$	V
Analog Output Pull-up Voltage	V_P	2.4		3.0	V
SO Pin 17 Output Pull-up Voltage	V_{OP}			$V+$	V
Frequency Compensation Capacitor (See Note)	C_{COMP}	0.01	0.1	1.0	μF

Note: Using a frequency compensation capacitor larger than 1 μF will promote low noise operation of the μPD7001C. However, the turn-on time at initial power on will increase.

AC Recommended Conditions

$T_A = 25°C \pm 2°C$;
$V+ = 5\ V \pm 0.25\ V$; Note 1

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Serial Mode						
Serial Clock Setup Time	t_{SKCS}	30			ns	$\overline{SCK}\uparrow \rightarrow \overline{CS}\downarrow$
CS Setup Time	t_{SCSK}	300			ns	$\overline{CS}\downarrow \rightarrow \overline{SCK}\uparrow$
Data Setup Time	t_{SIK}	120			ns	$SI \rightarrow \overline{SCK}\uparrow$
Data Hold Time	t_{HKI}	50			ns	$\overline{SCK}\uparrow \rightarrow SI$
High-Level Serial Clock Pulse Width	t_{WHK}	300			ns	
Low-Level Serial Clock Pulse Width	t_{WLK}	300			ns	
Strobe Hold Time	t_{HKST}	100			ns	$\overline{SCK}\uparrow \rightarrow \overline{STB}\uparrow$
High-Level Strobe Pulse Width	t_{WHST}	200			ns	
Low-Level Strobe Pulse Width	t_{WLST}	200			ns	
Chip Select Hold Time	t_{HKCS}	0			ns	$\overline{SCK}\uparrow \rightarrow \overline{CS}\uparrow$
Serial Clock Hold Time	t_{HCSK}	100			ns	$\overline{CS}\uparrow \rightarrow \overline{SCK}\downarrow$
Strobe Setup Time	t_{SSTCS}	300			ns	$\overline{STB}\uparrow \rightarrow \overline{CS}\downarrow$
Parallel Mode						
Address Setup Time	t_{AW}	0			ns	$\overline{CS}\downarrow \rightarrow \overline{WR}\downarrow$
Low-Level WR Pulse Width	t_{WW}	200			ns	
Address Hold Time	t_{WA}	0			ns	$\overline{WR}\uparrow \rightarrow \overline{CS}\uparrow$
Data Setup Time	t_{DW}	180			ns	$DB \rightarrow \overline{WR}\uparrow$
Data Hold Time	t_{WD}	0			ns	$\overline{WR}\uparrow \rightarrow DB$

Note: t_r, $t_f \leq 50$ ns.

AC Characteristics

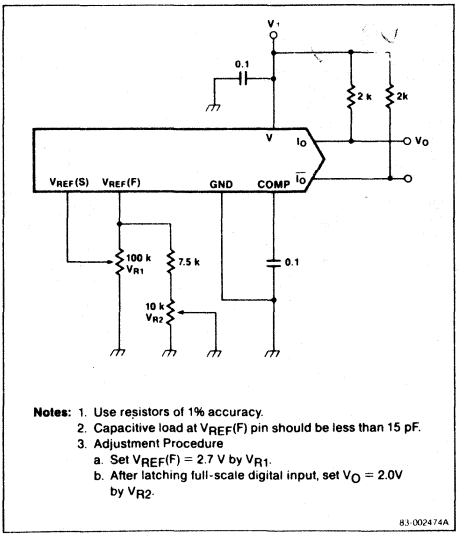
$T_A = 25°C \pm 2°C$; $V+ = +5\ V$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Analog Output Setting Time	t_{SET1}		1	3	μs	Parallel Mode, Note 1
	t_{SET2}		1	3	μs	Serial Mode, Note 2
Serial Data Delay Time	t_{DKO}			450	ns	$\overline{SCK}\downarrow \rightarrow SO$, Note 2
Delay Time T_D Floating S_O	t_{FCSO}			250	ns	$\overline{CS}\uparrow \rightarrow SO$, High Impedance

Notes: 1. $R_L \leq 2\ k\Omega$; $C_L \leq 20$ pF.
2. $R_L = 2\ k\Omega$; $C_L \leq 20$ pF.

Typical Applications

Connection Diagram



Notes: 1. Use resistors of 1% accuracy.
2. Capacitive load at $V_{REF}(F)$ pin should be less than 15 pF.
3. Adjustment Procedure
   a. Set $V_{REF}(F) = 2.7$ V by V_{R1}.
   b. After latching full-scale digital input, set $V_O = 2.0$V by V_{R2}.

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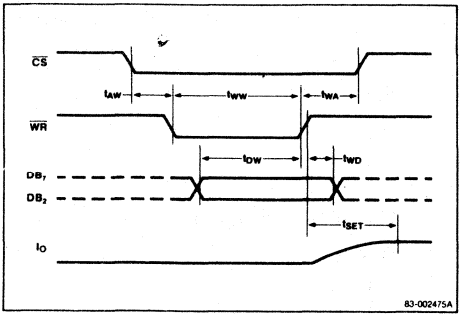
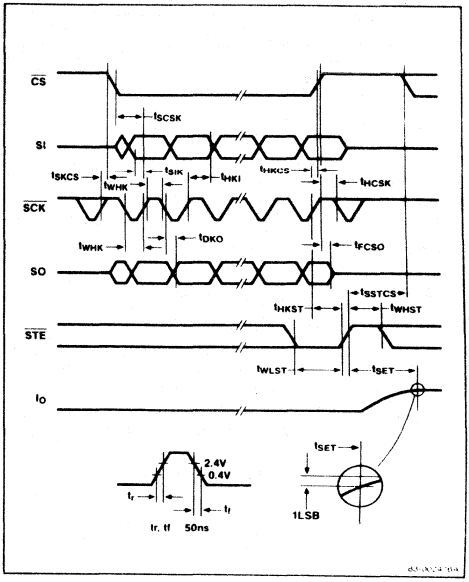
Timing Waveforms

Parallel Mode

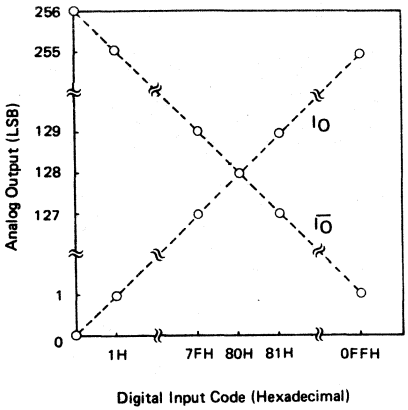


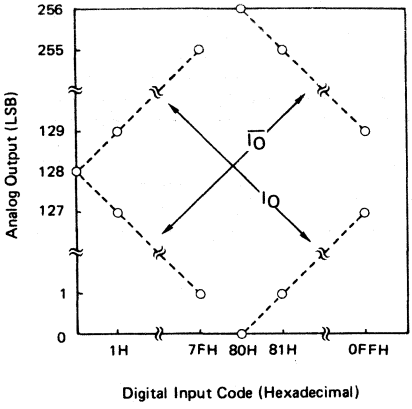
Serial Mode



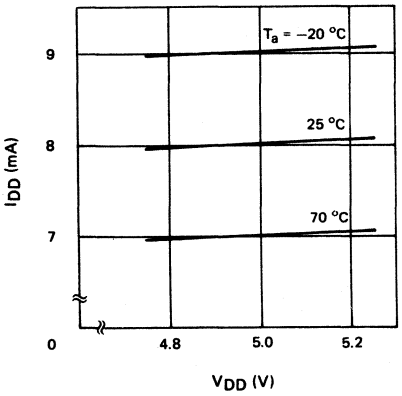
TYPICAL CHARACTERISTICS (T_a = 25°C)

IDEAL TRANSFER CHARACTERISTICS (BINARY CODE)

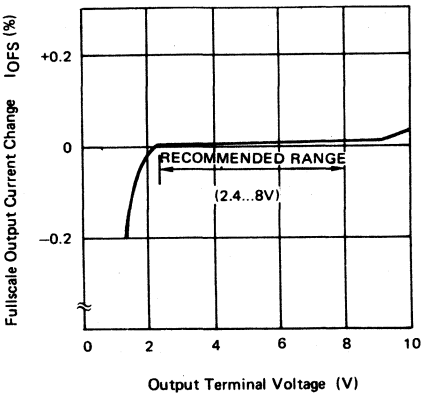




SUPPLY VOLTAGE CURRENT CHARACTERISTICS



FULLSCALE OUTPUT COMPLIANCE



EXTENDED TEMPERATURE RANGE

ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C

Operating Temperature	−40°C ... +85°C
Storage Temperature	−65°C ... +125°C
All Input Voltages	−0.3 ... V_{DD} +0.3 Volts
Power Supply	−0.3 ... +7 Volts
Power Dissipation	300 mW
SO Pin Pull-up Voltage	V_{DD} +0.3 Volts
IO/$\overline{IO}$ Pin Output Pull-up Voltage	+10 Volts

* COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent demage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Resolution		8	8	8	Bits	
Non Linearity 7011C	'N. L.		0.5	2	LSB	
Gain Error 7011C				10	%FSR	②
Fullscale Symmetry		−2	−1.0	0	LSB	③
Reference Voltage	V_{REF} (S)	1.41	2.0	2.59	V	
Power Supply Current	I_{DD}		8	20	mA	
Analog Output Compliance		2.4		8.0	V	$\Delta I_{OFS} < 2$ LSB
Logic Input Leakage	I_L		0.1	20	μA	V_I = 0 ... V_{DD}
Low Level Output Voltage	V_{OL}			0.7	V	$I_{SINK} < 2$ mA
Output Leakage	I_{OH}		0.1	20	μA	SO (PIN) 17), $V_O = V_{DD}$
Supply Voltage Rejection Ratio 7011C	SVR			2.0	%FSR/V	$\partial I_{FS} / \partial V_{DD}$
Low Level Logic Input	V_{IL}			0.5	V	
High Level Logic Input	V_{IH}	2.5			V	

②: Gain Error is defined as follows, 100 (I_{OFS} x 256/255 − 4 I_{REF}) / 4 I_{REF}
③: Fullscale Symmetry is defined as follows, 255 (I_{OFS} − $\overline{I_{OFS}}$) / I_{OFS}

Description

The μPD6950 is an 8-bit A/D converter for video signals. Although it is a CMOS converter (V+ = 5 V), its conversion rate is very high because a high-speed CMOS processing technique and full-parallel (flash) conversion method are used.

With its low power consumption and conversion rate of 20 Msps, this converter can be applied to various units such as digital video processing systems and high-speed fascimiles.

Features

- ☐ Resolution: 8 bits
- ☐ Conversion rate: 20 Msps (V+ = 5 V)
- ☐ Linearity: ±1/2 LSB typ
- ☐ Reference voltage: 3.5 V typ
- ☐ Power supply: 5 V single
- ☐ Low power consumption (350 mW typ)
- ☐ Available in 24 lead DIP

Absolute Maximum Ratings

T_A = 25°C

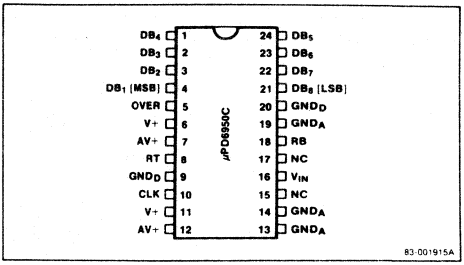
Power Supply Voltage	−0.3 to +7.0V
Input/Output Terminal Voltage	−0.3 to V_{DD}+0.3V
Analog GND Voltage	−0.3 to V_{IN} +0.3V
Reference GND Voltage	−0.3 to +0.3V
Operating Temperature Range	−20 to +75°C
Storage Temperature Range	−40 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ordering Information

Part Number	Package	Operating Temperature Range
μPD6950C	Plastic DIP	−20°C to +75°C

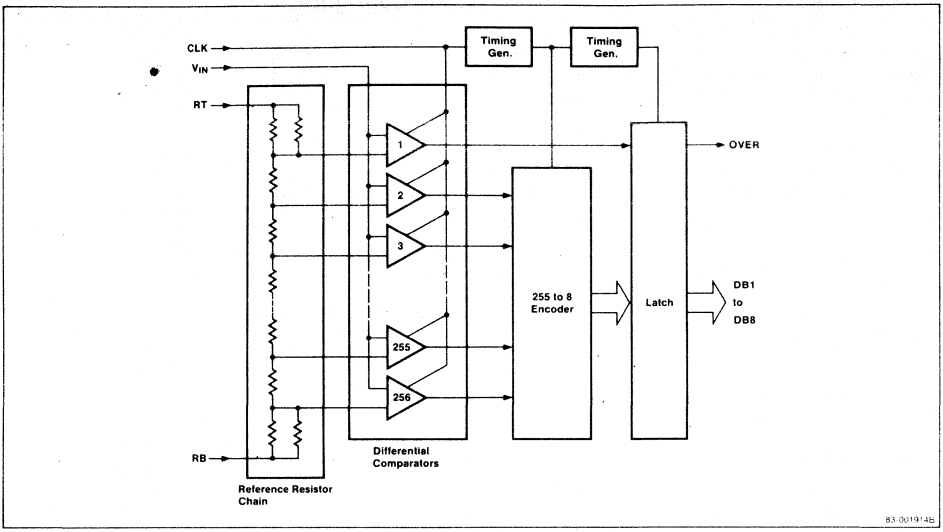
Pin Configuration



Pin Identification

Pin	Symbol	Function
1	DB_4	Digital output 4th
2	DB_3	Digital output 3rd
3	DB_2	Digital output 2nd
4	DB_1	Digital output MSB
5	OVER	Overrange
6	AV+	Analog power supply
7	V+	Power supply
8	RT	Reference voltage (high voltage side)
9	GND_D	Digital GND
10	CLK	Clock input
11	V+	Power supply
12	AV+	Analog power supply
13	GND_A	Analog GND
14	GND_A	Analog GND
15	NC	No connection
16	VIN	Analog input
17	NC	No connection
18	RB	Reference voltage (low voltage side)
19	GND_A	Analog GND
20	GND_D	Digital GND
21	DB_8	Digital output LSB
22	DB_7	Digital output 7th
23	DB_6	Digital output 6th
24	DB_5	Digital output 5th

Block Diagram



Electrical Characteristics

T_A = 25°C, V+ = AV+ = 5V, sampling rate = 20 MHz

Item	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Current Consumption	I_{DD}		50		mA	
Resolution	RES		8		bit	
Non-Linearity	NL			1.5	LSB	V_{REF} = 3.5V
Differential Gain	DG			5	%	f_{SAMP} = 14.318 MHz
Differential Phase	DP			5	°	f_{SAMP} = 14.318 MHz
Reference Resistance	R_{ref}		1.5		kΩ	
Data Output High-Level Current	I_{OH}			1.0	mA	V_{OH} = 2.5V
Data Output Low-Level Current	I_{OL}	1.8			mA	V_{OL} = 0.4V

Recommended Operating Conditions

T_A = 25°C

Item	Symbol	Limit Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Voltage	V+, AV+	4.5	5.0	5.5	V	
Reference Voltage	V_{REF}	2.5	3.5	3.5	V	
Sampling Clock	f_{SAMP}			20	MHz	
CLK Input High Level	V_{IH}	2.7			V	
CLK Input Low Level	V_{IL}			0.4	V	
Output Code			Binary			

Pin Functions

DB_1 to DB_8

DB_1 to DB_8 are the 8-bit digital signal output terminals. The analog signal input to terminal 16 (analog input terminal) is converted and sent from these terminals as an 8-bit digital signal. DB_1 corresponds to MSB, and DB_8 corresponds to LSB.

OVER

OVER is the overflow output terminal. When the analog input level (terminal 16) exceed the value of V_{OVER}, a high level is sent from this terminal.

(V_{OVER} = (255 + 1/2) LSB, 1LSB = $(V_{RT}-V_{RS})/256$

CLK

CLK is the A/D conversion clock input terminal. The analog data is latched on the rising edge of this clock. The internal encoder and latch circuit operations are synchronized with the timing pulses generated by this clock.

VIN

VIN is the analog input terminal. The analog signal to this terminal is converted on the rising edge of the CLK input clock and is sent from terminals DB_1 to DB_8 as an 8-bit digital signal.

RT

RT is the reference voltage input terminal on the high voltage side. It is the V_{REF} input terminal.

RB

RB is the reference voltage input terminal on the low voltage side. Normally, 0V is applied to this terminal.

AV+

AV+ is the power supply terminal for an analog system.

V+

V+ is the power supply terminal for a digital system.

GND_A

GND_A is the ground terminal for an analog system.

GND_D

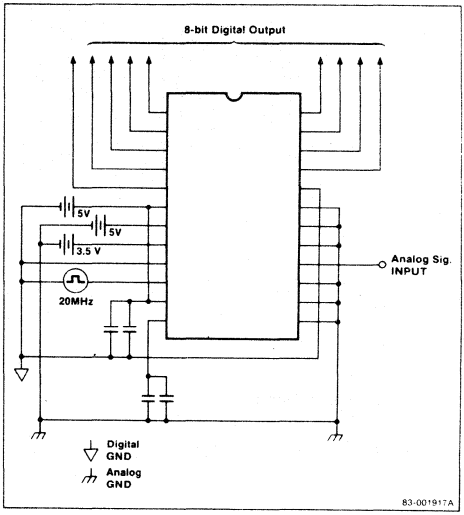
GND_D is the ground terminal for a digital system.

NC

NC is a non-connection terminal, but normally, it is connected to GND_A.

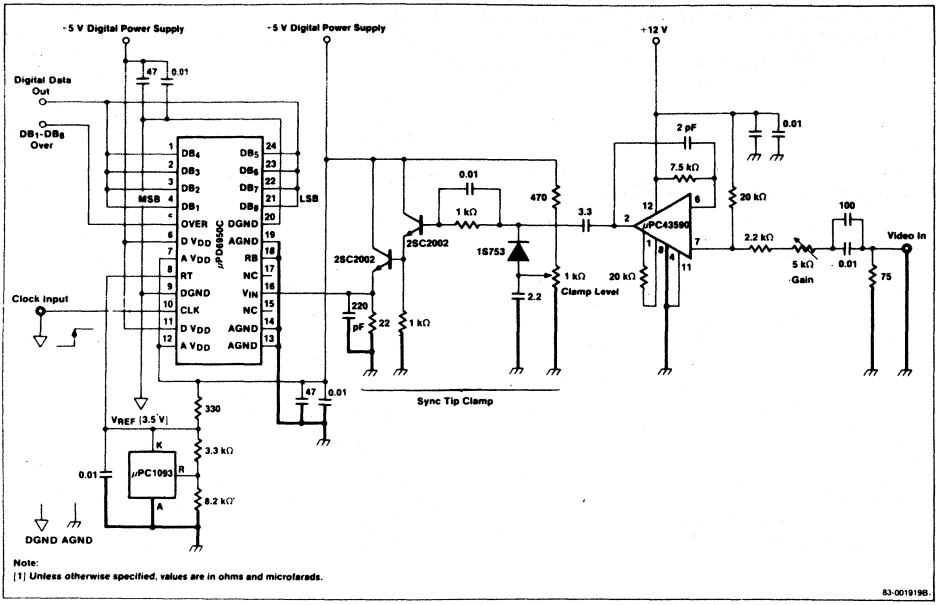
Typical Applications

Test Circuit

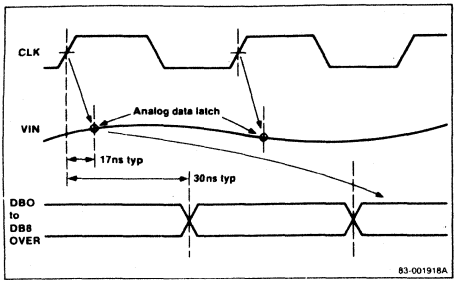


Typical Applications (Cont.)

Application Circuit



Timing Waveform



Output Data Format

Analog input	Digital output								
	OVER	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
V_{RB} to 1/2 LSB	0	0	0	0	0	0	0	0	0
1/2 LSB to 1 + 1/2 LSB	0	0	0	0	0	0	0	0	1
254 + 1/2 LSB to 255 − 1/2 LSB	0	1	1	1	1	1	1	1	1
255 + 1/2 LSB to V_{RT}	1	1	1	1	1	1	1	1	1
V_{RT} to V+	1	1	1	1	1	1	1	1	1

$$LSB \fallingdotseq \frac{V_{RT} - V_{RB}}{256}$$

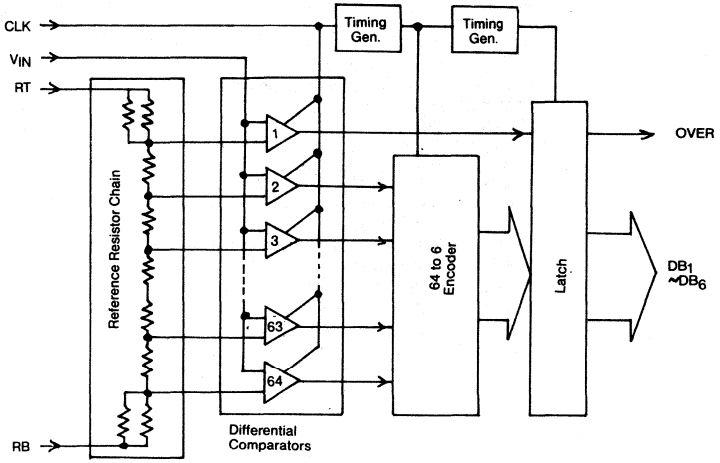
6-bit A/D converter CMOS

The μPD6951C is an 6-bit A/D converter for video signal.
Although it is a CMOS converter (V_{DD} = 5V), its conversion rate is very high because a high-speed CMOS technique and a full-parallel (flash) conversion method are used.
With its low power comsumption and conversion rate of 20Msps, this converter can be applied to various units such as digital video processing systems and high-speed facsimiles.

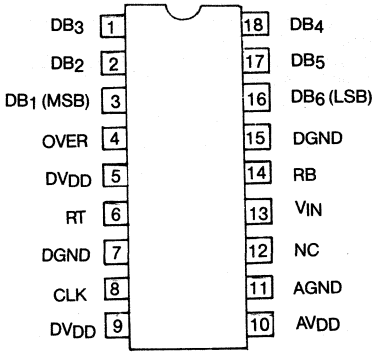
Features

- Resolution: 6 bits
- Conversion rate: 20Msps
- Linearity: ±1/2 LSB
- Reference voltage: 2.5 V TYP.
- Power supply voltage: +5V single
- Low power comsumption (125mW TYP.)
- TTL compatible (Digital output)
- 18 pin plastic DIP

Block Diagram



Connection Diagram (Top View)



1	DB_3	Digital output (3rd)
2	DB_2	Digital output (2nd)
3	DB_3	Digital output (MSB)
4	OVER	Over range
5	DV_{DD}	Digital power supply
6	RT	Reference voltage (high voltage side)
7	DGND	Digital GND
8	CLK	Clock input
9	DV_{DD}	Digital power supply
10	AV_{DD}	Analog power supply
11	AGND	Analog GND
12	NC	No connection
13	V_{IN}	Analog input
14	RB	Reference voltage (low level side)
15	DGND	Digital GND
16	DB_6	Digital input (LSB)
17	DB_5	Digital input (5th)
18	DB_4	Digital input (4th)

Pin Discription

Symbol	Function
DB_1–DB_6	DB_1 to DB_6 are the 6-bit digital signal output terminals. The analog signal input to terminal 13 (V_{IN}) is converted and output from these terminals as an 6-bit digital signal. DB_1 corresponds to MSB, and DB_6 corresponds to LSB.
OVER	OVER is the overflow output terminal. The analog input level exceeds the value of V_{OVER}, a high level is output from this terminal. (V_{OVER} = (63 + 1/2) LSB, 1LSB = (V_{RT}–V_{RB}) /64)
CLK	CLK is the A/D conversion clock input terminal. The analog data is latched on the rising edge of the clock. The internal encoder and latch circuit operations are synchronized with the timing pulses generated by this clock.
V_{IN}	V_{IN} is the analog input terminal. The analog input from this terminal is converted on the rising edge of the CLK input, and is output from terminals (DB_1–DB_6) as an 6-bit digital signal.
RT	RT is the reference voltage input terminal on the high voltage side. It is the V_{REF} input terminal.
RB	RB is the reference voltage input terminal on the low voltage side. Normally, 0 V is input to this terminal.
AV_{DD}	AV_{DD} is the power supply terminal for an analog system. Normally, +5 V is input to this terminal.
DV_{DD}	DV_{DD} is the power supply terminal for a digital system. Normally, +5 V is input to this terminal.
AGND	AGND is the ground terminal for an analog system.
DGND	DGND is the ground terminal for a digital system.
NC	NC is a non-connection terminal.

Absolute Maximum Ratings (T_a = 25°C)

Parameter	Rating	Unit
Power supply voltage	−0.3 to +7.0	V
Input terminal voltage	−0.3 to V_{DD} +0.3	V
Output terminal voltage	−0.3 to V_{DD} +0.3	V
Reference GND voltage	−0.3 to +0.3	V
Operating temperature range	−10 to +75	°C
Strage temperature range	−40 to +125	°C

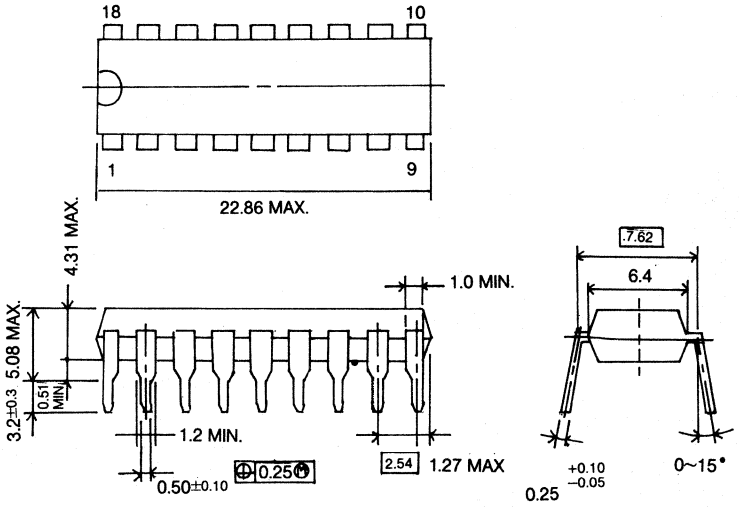
Recommended Operating Condition (T_a = 25°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}		4.5	5.0	5.5	V
Reference voltage	V_{REF}		2.0	2.5	3.5	V
Sampling clock	f_{samp}				20	MHz
CLK input high level	V_{IH}		2.7			V
CLK input low level	V_{IL}				0.4	V

Electrical Characteristics (T_a = 25°C, V_{DD} = 5V, f_{samp} = 20MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD}			25		mA
Resolution	RES			6		bit
Non-linearity	NL				±1/2	LSB
Differential gain	DG			2		%
Differential phase	DP			2		°
Reference registance	R_{REF}			0.5		kΩ
Data output high level voltage	V_{OH}	I_{OH} = −1.0mA	2.8			V
Data output low level voltage	V_{OL}	I_{OL} = 1.8mA			0.4	V

Package Dimensions (Unit : mm)
18 pin plastic DIP (300 mil)



Description

The μPD7001 is a high performance, low power, 8-bit CMOS analog-to-digital converter. Using the Successive Approximation Register (SAR) technique, the 7001 offers the designer the convenience of serial data output and microprocessor interface, with the versatility of four addressable multiplexed analog inputs and low power CMOS operation.

Features

- ☐ 4 channel multiplexed analog input
- ☐ Auto zero and full scale correction without external components
- ☐ Serial data output
- ☐ High input impedance 1000 MΩ
- ☐ Operates from a single +5 V supply
- ☐ Low power operation (CMOS)
- ☐ 140 μs conversion speed
- ☐ Linearity: 0.8% FSR

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7001C	Plastic DIP	0°C to +70°C

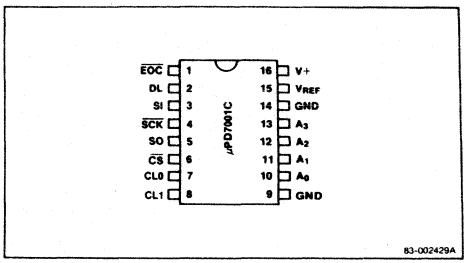
Absolute Maximum Ratings

$T_A = 25°C$

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to 125°C
Analog Input Voltage	−0.3 V to V+ + 0.3 V
Reference Input Voltage	−0.3 V to V+ + 0.3 V
Digital Input Voltage	−0.3 V to +12 V
Maximum Pull-up Voltage	+12 V
Supply Voltages	−0.3 V to +7 V
Power Dissipation	200 mW

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

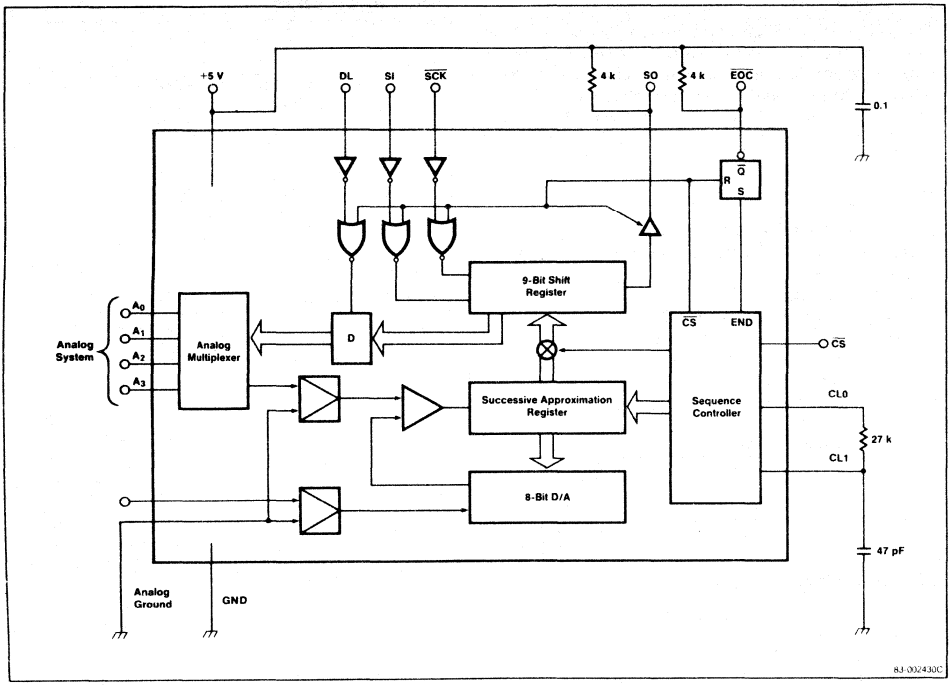
Pin Configuration



Pin Identification

Pin	Name	Symbol	Function
1	End of Conversion	EOC	High impedance when $\overline{CS}$ = Low. Open drain output.
2	Data Latch	DL	MPX addresses are latched at the falling edge of DL input.
3	Serial Input	SI	Pin to accept MPX address data. Data read at the rising edge of $\overline{SCK}$ input.
4	Serial Clock	$\overline{SCK}$	$\overline{SCK}$ controls the shift operation of I/O interface 8-bit shift register. Input.
5	Serial Output	SO	Conversion data in shift register are output at the falling edge of $\overline{SCK}$. High impedance when $\overline{CS}$ = High. Open drain output.
6	Chip Select	$\overline{CS}$	$\overline{CS}$ = High: A/D conversion mode $\overline{CS}$ = Low: Interface mode. Input.
7	Clock	CL0	Pin for clock oscillation.
8	Clock	CL1	Pin for clock oscillation.
9	Digital Ground	V_{SS}	Ground terminal. Tie to GND with analog GND externally.
10-13	Analog Inputs	A_0 to A_3	Analog input terminals.
14	Analog GND	GND	Ground terminal for analog inputs and references.
15	Reference Input	V_{REF}	Pin to set full scale voltage. $V_{REF} \sim 2.5$ V.
16	Power Supply	V+	+5 V

Block Diagram



DC Characteristics

$T_A = +25°C \pm 2°C$; $f_{clk} = 400$ kHz; V+ = 5 V, ±0.25 V, $V_{REF} = 2.500$ V, Note 1

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution				8	Bit	
Nonlinearity	NL			0.8	%FSR	
Full-Scale Error			1	2	LSB	
Full-Scale Error Temperature Coefficient			30		ppm/°C	
Zero Error				2	LSB	
Zero Error Temperature Coefficient			30		ppm/°C	
Total Unadjusted Error 1	TUE1			2	LSB	Note 4
Total Unadjusted Error 2	TUE2			2	LSB	Note 5
Analog Input Voltage	V_{IN}	0		V_{REF}	V	Note 1
Analog Input Resistance	R_{IN}		1000		MΩ	$V_I = 0$ to V
Conversion Time	t_{CONV}		140		μs	Note 2
Clock Frequency Range	f_{clk}*	0.01	0.4	0.5	MHz	
Clock Frequency Distribution	Δf_{clk}		±5	±20	%	R = 27 KΩ, C = 47 pF, f_{CK} = 400 kHz
Serial Clock Frequency	f_{SCK}		0.5		MHz	Note 3
High Level Voltage	V_{IH}	3.6			V	
Low Level Voltage	V_{IL}			1.4	V	
Digital Input Leakage Current	I_{ILK}		1.0	10	μA	$V_I = V_{SS}$ to +10 V
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 1.7$ mA
Output Leakage Current	I_{OLK}		1.0	10	μA	$V_O = +10$ V
Power Dissipation	P_D		5	15	mW	

Notes: 1. All digital outputs are put at a high level when $V_I > V_{REF}$.

2. A/D conversion is started with $\overline{CS}$ going high; at the final step of the first A/D conversion, $\overline{EOC}$ is low. The conversion time is:

$$t_{CONV} = 56/f_{CK}$$

3. For $f_{SCK} < 500$ kHz, the load capacitor (stray capacitance included) and the pull-up resistor, which are connected to serial output, are required to be not more than 30 pF and 4 kΩ respectively.
4. V+ = 5.0 V, $V_{REF} = 2.5 \pm 0.25$ V.
5. V+ = 4.5 to 5.5 V.

AC Characteristics

$T_A = +25°C \pm 2°C$; $f_{clk} = 400$ kHz; V+ = 5 V, Note 1

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}$ to $\overline{CS}$
$\overline{CS}$ Setup Time	t_{SCSK}	12.5			μs	$\overline{CS}$ to $\overline{SCK}$ Note 1
Address Data Setup Time	t_{SIK}	150			ns	
Address Data Hold Time	t_{HKI}	100			ns	
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	
Low Level Serial Clock Pulse Width	t_{WCK}	400			ns	
Data Latch Hold Time	t_{HKDL}	200			ns	$\overline{SCK}$ to DL
Data Latch Pulse Width	t_{DKO}	200			ns	
Serial Data Delay Time	t_{DKO}			500	ns	$\overline{SCK}$ to SO. $R_L = 3$ K (Note 2), $C_L = 30$ pF
Delay Time to Floating SO	t_{FCSO}			250	ns	$\overline{CS}$ to High Impedance SO
$\overline{CS}$ Hold Time	t_{HKCS}	200			ns	

Notes: 1. When $\overline{CS}$ is high, the μPD7001 performs A/D conversion and does not accept any external digital signal. It remains at the previous state continuously. When $\overline{CS}$ is low, the data is exchanged with the external digital circuits. However, 5 internal clock pulses are needed before digital data is output. The rating corresponds to the 5 clock signal pulses:

$$t_{SCSK}\ (min) = 5/f_{clk}$$

2. The serial data delay time depends on load capacitance and pull-up resistance: $t_{DKO} = 2.3 \times R_L \times C_L + 100$ ns.

Addressing the Inputs

One of the four analog inputs is selected by toggling the chip select line at pin 6 "low" and presenting a 2-bit serial code (from the host controller) to the Serial Input (SI) at pin 3.

The "channel select" data is sent to the upper 2 bits of the 9-bit shift register on the rising edge of the Serial Clock ($\overline{SCK}$) at pin 4 and loaded into the Data Latch on the falling edge of the Data Latch signal at pin 2.

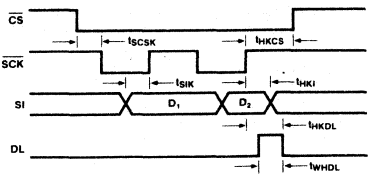
Referring to figure 1 the analog input addressing sequence is:

- ☐ Chip Select ($\overline{CS}$ pin 6) toggled "low" or 0
- ☐ 2-bit "channel select" data presented to SI and pin 3
- ☐ Data shifted in on $\overline{SCK}$ rising edge
- ☐ Data Latch signal present at pin 2 (pulse is 200 ns min.)
- ☐ Mux address data latched on falling edge of DL signal.

Multiplexer Channel Selection

Input	D0	D1
A0	Low	Low
A1	High	Low
A2	Low	High
A3	High	High

Figure 1. Analog Channel Selection



Note: Addressing the μPD7001 inputs can be implemented simultaneously with Serial Data Output.

Rise and Fall times of all signals should not exceed 50 ns.

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The Conversion Process

When Chip Select ($\overline{CS}$) at pin 6 is "high," all external inputs (except the selected analog input) and outputs are disabled and the internal Sequence Controller controls the conversion process on the selected analog input via the A/D converter section.

The A/D converter section is comprised of the comparator and buffer amplifier, the successive approximation register and an 8-bit digital to analog (D/A) converter. Because the SAR technique requires the input voltage be stable during the conversion process, it is recommended that a low pass filter and a sample and hold circuit precede the analog input. Failure to present stable input voltage will result in conversion errors.

A single conversion requires 56 internal clock periods, which are clock periods generated by the Sequence Controller Clock (CL0) and CL1 at pins 7 and 8 respectively. The internal clock speed is set by Rcl and Ccl and the values shown in figure 2 are recommended for proper timing.

The final step in the conversion process is the transfer of converted data to the shift register and signaling (to the external controlling device) that the converted data is available for reading, via the End of Conversion ($\overline{EOC}$) pulse at pin 1.

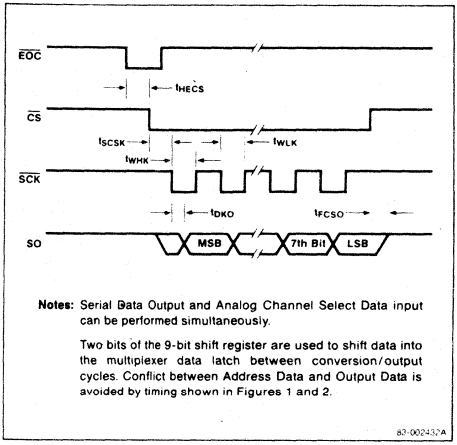
If the data is not to be read then the Chip Select ($\overline{CS}$) line is kept in the "high" state and the Sequence Controller begins the next conversion of the last selected analog channel. Note again that "channel select" data and "converted" data output can only be initiated while the Chip Select line is "low." The sequence of data conversion and output is shown in figure 2.

Sequence:

- ☐ Analog channel selection (1 of 4):
  $\overline{CS}$ = "low"
- ☐ Analog-to-digital conversion (internal):
  $\overline{CS}$ = "high"
- ☐ Internal load of "converted data" to shift register (56 internal clock cycles):
  $\overline{CS}$ = "high"
- ☐ $\overline{EOC}$ signals data ready to external controller:
  $\overline{CS}$ = "high"
- ☐ Output of serial data to controlling device and/or refresh of analog input select data:
  $\overline{CS}$ = "low"

Stability of the analog input voltage level is critical to the conversion accuracy of the μPD7001, as with any SAR type converter, during the conversion cycle. When $\overline{CS}$ is "high," the converter responds to whatever voltage level is present at the selected input. For DC level sampling from remote sensors a low pass filter (similar to that shown in figure 3) and a sample and hold circuit (such as the μPC398) is recommended.

Figure 2. Digital Data Output

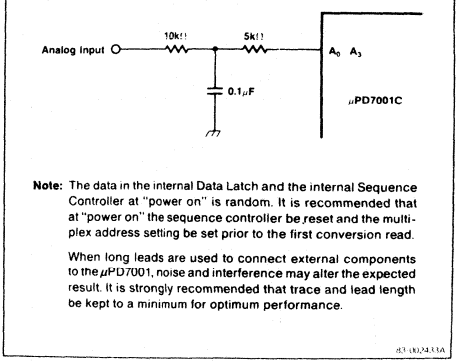


Notes: Serial Data Output and Analog Channel Select Data input can be performed simultaneously.

Two bits of the 9-bit shift register are used to shift data into the multiplexer data latch between conversion/output cycles. Conflict between Address Data and Output Data is avoided by timing shown in Figures 1 and 2.

83-002437A

Figure 3. Low Pass Filter Circuit



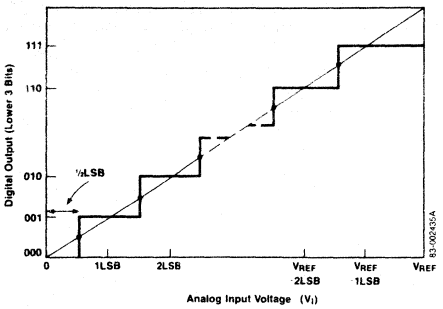
Note: The data in the internal Data Latch and the internal Sequence Controller at "power on" is random. It is recommended that at "power on" the sequence controller be reset and the multiplex address setting be set prior to the first conversion read.

When long leads are used to connect external components to the μPD7001, noise and interference may alter the expected result. It is strongly recommended that trace and lead length be kept to a minimum for optimum performance.

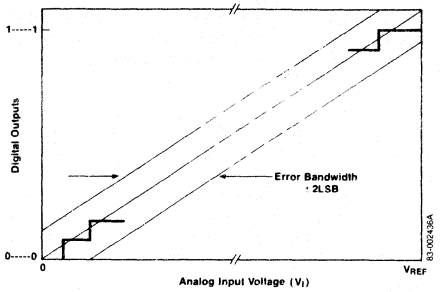
83-002433A

Operating Characteristics

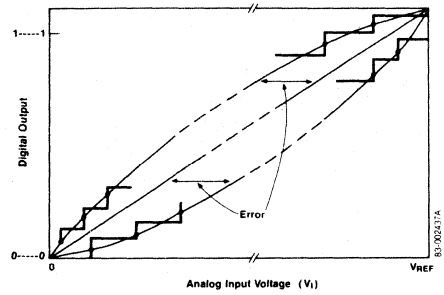
Ideal Input/Output Transfer Characteristics



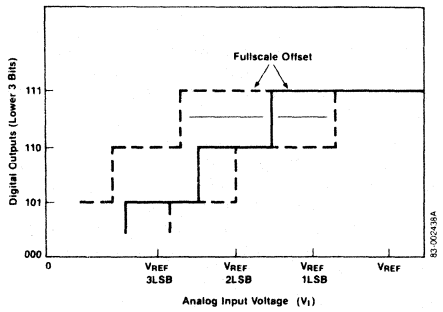
Total Unadjusted Error



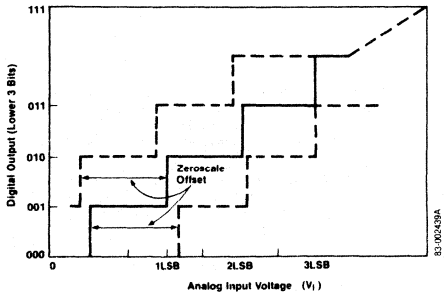
Linearity Error



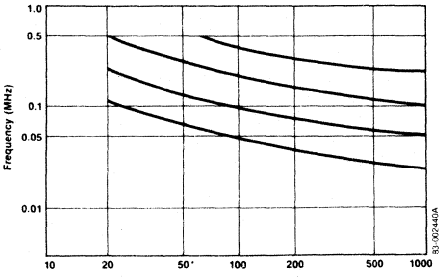
Full Scale Error



Zero Scale Error

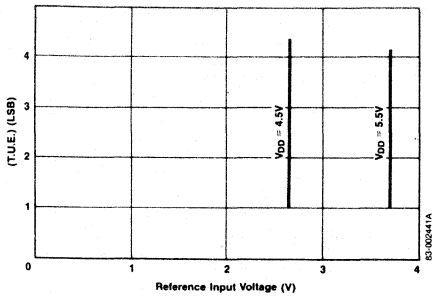


Clock Frequency Range

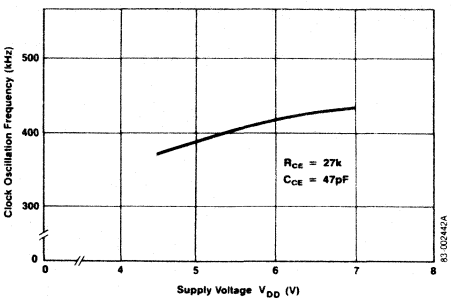


Operating Characteristics (Cont.)

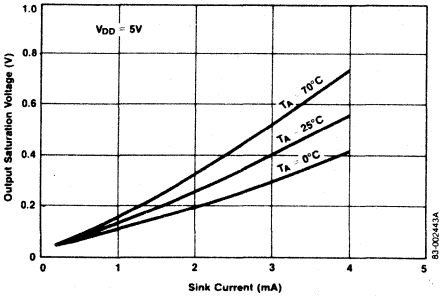
Total Unadjusted Error vs. V_{REF}



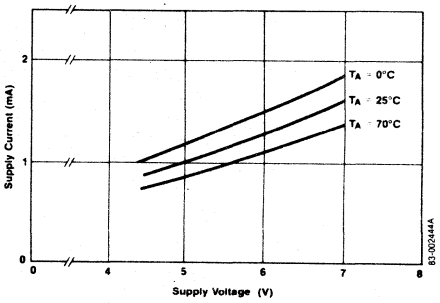
Clock Oscillation Frequency vs. Current Characteristics



Output Sink Current vs. Saturation Voltage Characteristics



Supply Voltage vs. Current Characteristics



EXTENDED TEMPERATURE RANGE

DC CHARACTERISTICS

T_a = –40°C ... +110°C; V_{DD} = +5V ± 5 %; V_{REF} = 2.5V; f_{CK} = 200 kHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Resolution			8	8	Bit	V_{DD} = 5V V_{REF} = 2.25 ... 2.75V
Non Linearity				1.2	% FSR	V_{DD} = 5V V_{REF} = 2.25 ... 2.75V
Full-Scale Error				3	LSB	V_{DD} = 5V V_{REF} = 2.25 ... 275V
Full-Scale Error Temp. Coefficient			30		ppm/°C	V_{DD} = 5V V_{REF} = 2.25 ... 2.75V
Zero Error				3	LSB	V_{DD} = 5V V_{REF} = 2.25 ... 2.75V
Zero Error Temp. Coefficient			30		ppm/°C	V_{DD} = 5V V_{REF} = 2.25 ... 275V
Total Unadjusted Error 1	T.U.E 1			3	LSB	V_{DD} = 5V V_{REF} = 2.25 ... 2.75V
Total Unadjusted Error 2	T.U.E. 2			3	LSV	V_{DD} = 4.5V ... 5.5V V_{REF} = 2.500V
Analog Input Voltage	V_I	0		V_{REF}	V	
Analog Input Resistance	R_I		1000		MΩ	V_I = 0 to V_{DD}
Conversion Time	tCONV		280		μs	
Clock Frequency Range	f_{CK}	Q 1	Q 2	0.3	MHz	
Clock Frequency Distribution	f_{CK}		± 15	± 30	%	R = 68KΩ, C = 47pF (f_{CK} = 0.2MHz)
Serial Clock Frequency	f_{SCK}		0.5		MHz	
High Level Voltage	V_{IH}	3.8			V	
Low Level Voltage	V_{IL}			1.2	V	
Digital Input Leakage Current	I_I			15	μA	V_{ID} = V_{SS} to +10V
Low Level Output Voltage	V_{OL}			0.8	V	I_{OL} = 1.7mA
Output Leakage Current	I_L			15	μA	V_O = +10V
Power Dissipation	P_d		7	20	mW	

AC CHARACTERISTICS

T_a = –40°C ... +110°C; f_{CK} = 200 kHz; V_{DD} = 5V ± 5 %

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
$\overline{EOC}$ Hold Time	tHECS	0			μs	$\overline{EOC}$ to $\overline{CS}$
$\overline{CS}$ Setup Time	tSCSK	25			μs	$\overline{CS}$ to $\overline{SCK}$
Address Data Setup Time	tSIK	150			ns	
Address Data Hold Time	tHKI	100			ns	
High Level Serial Clock Pulse Width	tWHK	400			ns	
Low Level Serial Clock Pulse Width	tWLK	400			ns	
Data Latch Hold Time	tHKDL	200			ns	$\overline{SCK}$ to DL
Data Latch Pulse Width	tWHDL	200			ns	
Serial Data Delay Time	tDKO			600	ns	$\overline{SCK}$ to SO, R_L = 3KΩ CL = 30pF
Delay Time to Floating SO	tFCSO			300	nd	$\overline{CS}$ to High impedance SO
$\overline{CS}$ Hold Time	tHKCS	200			ns	

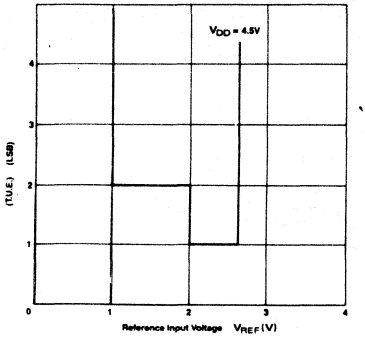
THERE IS A RESTRICTION TO THE USE OVER – 40 TO PLUS 110 DEG C TEMP RANGE. HERE IS THE RESTRICTION.

IN CASE THAT THERE IS A PAUSE PERIOD OF MORE THAN 10 MSEC BETWEEN ONE CONVERSION AND THE OTHER, A DUMMY CONVERSION IS REQUIRED IN BETWEEN AS SHOWN IN THE FOLLOWING FIGURE.

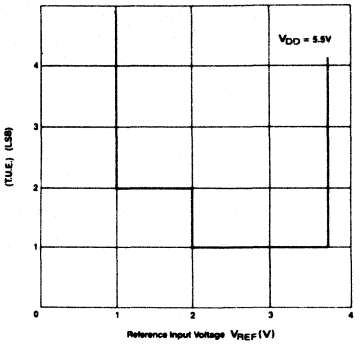
THIS DUMMY CONVERSION CAN BE IMPLEMENTED BY WRITING A CONVERSION INSTRUCTION ONTO THE CONTROLLER PART. SINCE THE OUTPUT DATA OF THE DUMMY CONVERSION IS A MEANINGLES VALUE, THE READ OPERATION BY MICROCOMPUTER IS NOT NECESSARY.

THE REASON FOR THIS RESTRICTION IS AS FOLLOWS.

T_a = 25°C
T.U.E. VS. V_{REF}



T.U.E. VS. V_{REF}



APPLICATION HINTS

1. Data held in the internal sequence controller and address latch just after power-on is random. Therefore, an MPX address setting and a sequence controller resetting are required before a first conversion data reading.
2. When using long wires to connect external components and μPD7001 terminals, noise induction and some interference must be expected and taken into account.
3. The μPD7001 uses the successive approximation technique for A/D conversion; therefore, a sample and hold circuit is required when a fast varying analog input signal is applied. In addition, a C-R filter as shown below should be used, in order to minimize noise in a DC analog input signal.

APPLICATION EXAMPLE: REDUCING DIGITAL I/O TERMINALS

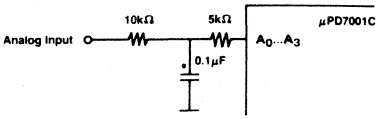
Please refer to the Block Diagram on page 2 and the Timing Waveforms on page 4.

In this application, an MPX address write is required in every Date Read.

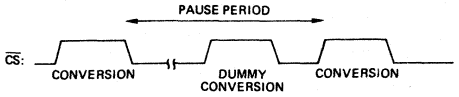
A wired OR connection is feasible, because $\overline{EOC}$ and SO are both open drain output and the signal output timing of $\overline{EOC}$ is different from that of SO.

The DL signal is strobed by $\overline{CS}$ in the chip. Therefore, by connecting DL to V_{DD}, MPX Address Data is latched at the rising edge of $\overline{CS}$.

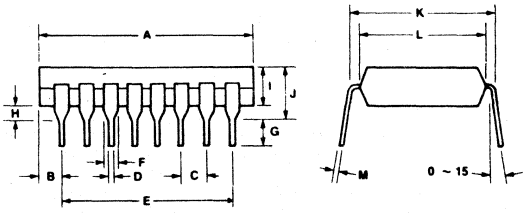
C-R Filter



WHEN THE 7001 IS IN PAUSE FOR A LONG TIME AT HIGH TEMP WITHOUT ANY CONVERSION INSTRUCTION, THE ANALOG CHARGE (OFFSET VOLTAGE COMPENSATION ETC.) RETAINED ON THE INTERNAL CAPACITORS CAN BE DISCHARGED. IN ORDER TO SECURE THE RETURN TO THE NORMAL OPERATION, A DUMMY CONVERSION MUST BE INSERTED.



PACKAGE OUTLINE
μPD7001C (Plastic)



ITEM	MILLIMETERS	INCHES
A	19.4 max	0.76 max
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 min	0.10 min
H	0.5 min	0.02 min
I	4.05 max	0.16 max
J	4.55 max	0.18 max
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

Description

The μPD7002 is a high performance, low power, 10-bit CMOS analog-to-digital converter. Using the integrating technique the 7002 offers the designer full microprocessor interface, four multiplexed analog inputs, and low power CMOS construction.

Features

- ☐ 8- or 10-bit resolution (selectable)
- ☐ 4 channel multiplexed analog input
- ☐ Auto zero and full scale correction without external components
- ☐ High input impedance — 1000 MΩ
- ☐ Internal status register can be accessed by host controller
- ☐ Operates from single +5 V supply
- ☐ Interfaces to most 8-bit microprocessors
- ☐ Low power operation (CMOS)
- ☐ 5 ms conversion speed (10 bits with f_{CK} = 2 MHz)
- ☐ Available in two performance ranges:
  Conversion accuracy (maximum with T_A = 0 to +50°C):
  μPD7002C-1 ..... 0.1% FSR
  μPD7002C ..... 0.2% FSR

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7002C	Plastic DIP	−20°C to +70°C

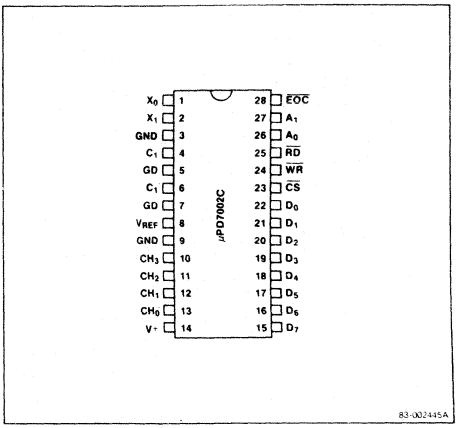
Absolute Maximum Ratings

T_A = +25°C

Operating Temperature	−20°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage	−0.3 V to +7.0 V
All Input Voltages	−0.3 V to V+ 0.3 V
Power Dissipation	300 mW
Analog GND Voltage	± 0.3 V

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

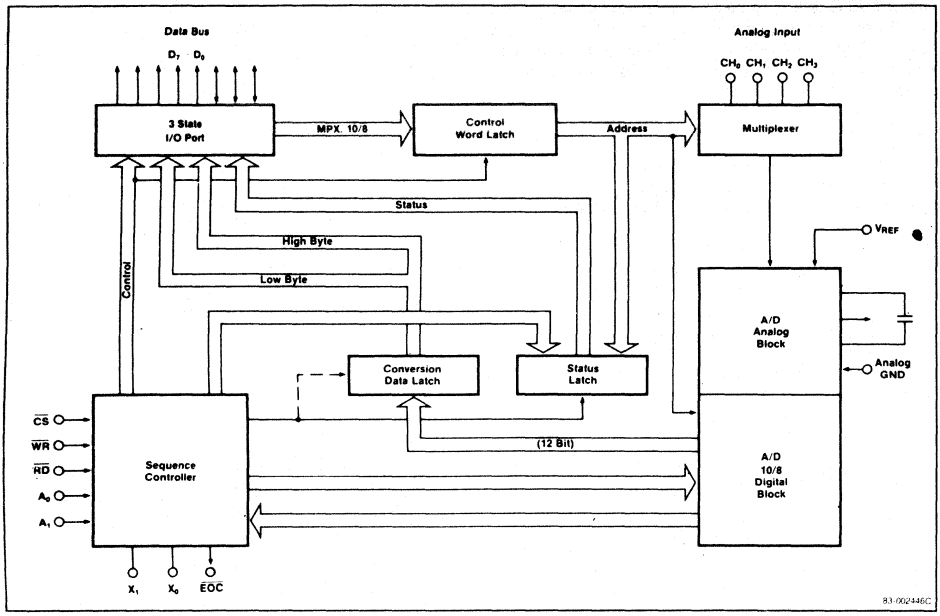
Pin Configuration



Pin Identification

Pin	Name	Function
1, 2	X_0, X_1	External clock input
3	GND	TTL ground
4, 6	CI	Integrating capacitor
5, 7	GD	Guard
8	V_{REF}	Reference voltage input
9	GND	Analog ground
10	CH_3	Analog channel 3
11	CH_2	Analog channel 2
12	CH_1	Analog channel 1
13	CH_0	Analog channel 0
14	V+	Voltage (+5 V)
15-22	D_7-D_0	Data bus
23	$\overline{CS}$	Chip select
24, 25	$\overline{WR}$, $\overline{RD}$	Control bus
26, 27	A_0, A_1	Address bus
28	$\overline{EOC}$	End of conversion interrupt

Block Diagram



Digital I/O Pin Function

Pin	Symbol	Name	I/O	Function
1, 2	X_0, X_1	Xtal	—	Xtal OSC. X_1 can be used as the input of external clock.
15–22	D_7–D_0	Data Bus	Three-state (1 TTL) I/O	A/D conversion data (High and Low Byte) and internal status output to 8-bit Data Bus. MPY Address, 8/10 select and flag data input from bus. High impedance when μPD7002 is not enabled ($\overline{CS}$ = High).
23	$\overline{CS}$	Chip Select	Input	Low level of $\overline{CS}$ makes other input pins ($\overline{WR}$, $\overline{RD}$, A_0, A_1) enable and data transmission and receiving are possible through data bus pins.
24	$\overline{WR}$	Write	Input	When $\overline{WR}$ = Low, μPD7002 receives new data from data bus.
25	$\overline{RD}$	Read	Input	When $\overline{RD}$ = Low, μPD7002 transmits conversion data and internal status to data bus.
26, 27	A_0, A_1	Address	Input	A_0, A_1 designate the data in data bus (High, Low, Status Byte).
28	$\overline{EOC}$	End of Conversion	Output (1 TTL)	$\overline{EOC}$ indicates the end of conversion to external chips. Read mode operation (high byte output) resetable $\overline{EOC}$.

DC Characteristics

$T_A = 0°C$ to $+50°C$; $V+ = +5\ V \pm 0.25\ V$
$V_{REF} = +2.50\ V$, $f_{clk} = 1\ MHz$, $C_{INT} = 0.033\ \mu F$, 10-Bit Mode

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution, 7002C-1		10	11	12	Bits	
Resolution, 7002C		9	11	12	Bits	
Nonlinearity, 7002C-1			0.05	0.1	%FSR	
Nonlinearity, 7002C			0.1	0.2	%FSR	
Full Scale Error, 7002C-1			0.05	0.1	%FSR	
Full Scale Error, 7002C			0.1	0.2	%FSR	
Zero Scale Error, 7002C-1			0.05	0.1	%FSR	
Zero Scale Error, 7002C			0.1	0.2	%FSR	
Full Scale Temperature Coefficient			10		ppm/°	
Zero Scale Temperature Coefficient			10		ppm/°C	
Analog Input Resistance	R_{IN}		1000		MΩ	$V_{IN} = 0$ to $V+$
Total Unadjusted Error 1, 7002C-1	TUE1		0.05	0.1	%FSR	
Total Unadjusted Error 1, 7002C	TUE1		0.1	0.2	%FSR	
Total Unadjusted Error 2, 7002C-1	TUE2		0.05	0.1	%FSR	
Total Unadjusted Error 2, 7002C	TUE2		0.1	0.2	%FSR	
Clock Input Current	I_{clk}		5	50	μA	X_I pin can be used as an external CMOS level clock input. When external clock is applied. X_O pin should be left open.
High Level Output Voltage	V_{OH}	$V+ - 1.5$			V	$I_O = -1.6\ mA$, $T_A = -20$ to $+70°C$
Low Level Output Voltage	V_{OL}			0.45	V	$I_O = 1.6\ mA$, $T_A = -20$ to $+70°C$
Digital Input Leakage Current	I_{ILK}		1	10	μA	$0 \le V_{IN} \le V+$
Output Leakage Current	I_{OLK}		1	10	μA	$0 \le V_{IN} \le V+$
Power Dissipation	P_D		15	25	mW	

AC Characteristics

T_A = +25°C; V+ = +5 V ± 0.25 V, V_{REF} = +2.5 V, f_{clk} = 1 MHz, C_{INT} = 0.033 μF

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Conversion Speed (10 bit)	t_{CONV}	8.5	10	15	ms	
Conversion Speed (8 bit)	t_{CONV}	2.4	4	5	ms	
Address Setup Time $\overline{CS}$, A_0, A_{11} to $\overline{WR}$	t_{AW}	50			ns	
Address Setup Time $\overline{CS}$, A_0, A11 to $\overline{RD}$	t_{AR}	50			ns	
Address Hold Time $\overline{WR}$ to $\overline{CS}$, A_0, A_1	t_{WA}	50			ns	
Address Hold Time $\overline{RD}$ to $\overline{CS}$, A_0, A_1	t_{RA}	50			ns	
Low Level $\overline{WR}$ Pulse Width	t_{WW}	400			ns	
Low Level $\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time Input Data to $\overline{WR}$	t_{DW}	300			ns	
Data Hold Time $\overline{WR}$ to Input Data	t_{WD}	50			ns	
Output Delay Time $\overline{RD}$ to Output Data	t_{RD}			300	ns	Note 1
Delay Time to High Z Output $\overline{RD}$ to Floating Output	t_{DF}			150	ns	

Note: 1 TTL load + 100 pF.

Recommended Operating Conditions

T_A = +25°C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	4.75	5.00	5.25	V	
Reference Voltage	V_{REF}	2.25	2.50	2.75	V	
Analog Input Voltage	V_{IN}	0		V_{REF}	V	Note 1
Clock Frequency	f_{clk}	0.5	1	3	MHz	Note 2
Integrating Capacitor	C_{INT}	0.029	0.033		μF	
High Level Input	V_{IH}	2.2			V	Note 3
Low Level Input	V_{IL}			0.8	V	Note 3
High Level Clock Input	V_{XHL}	V+ − 1.4			V	Note 3
Low Level Clock Input	V_{XLL}			1.4	V	Note 3

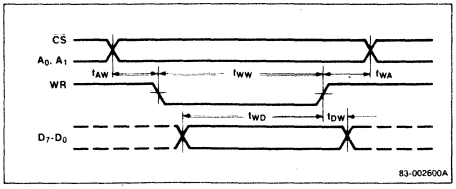
Notes: 1. Negative voltage input (< −0.2 V) decreases the input impedance. Furthermore, conversion error for the input through another MPX channel also increases.

Notes [Cont.]:

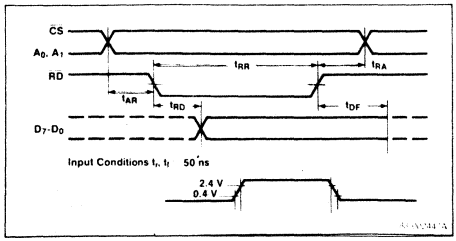
2. Integrating capacitor: C_{INT} depends on clock frequency and can be obtained as follows $C_{INT}(\mu F) = 0.033/f_{clk}$ (MHz). Note that conversion time is inversely proportional to the clock frequency.
3. T_A = −20°C to +70°C, V+ = +5 V ± 0.25 V.

Timing Waveforms

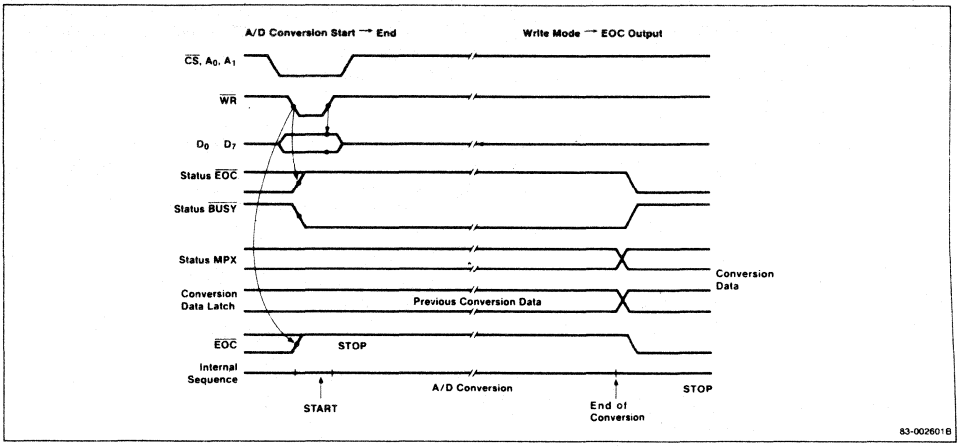
Write Mode



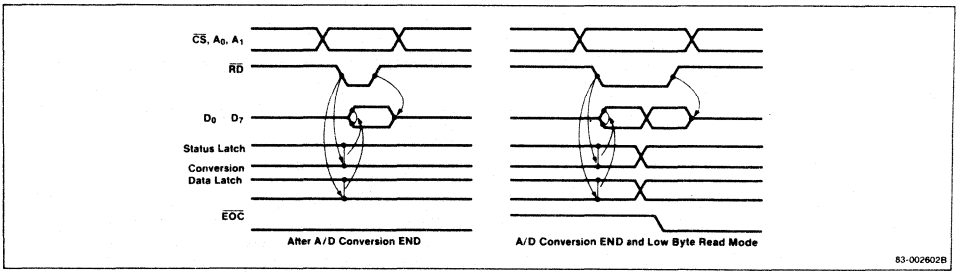
Read Mode



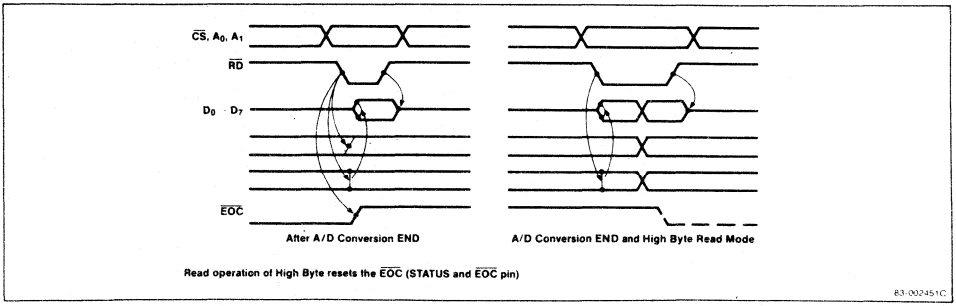
Timing Waveforms (Cont.)



Read Mode (Status, Low Byte)



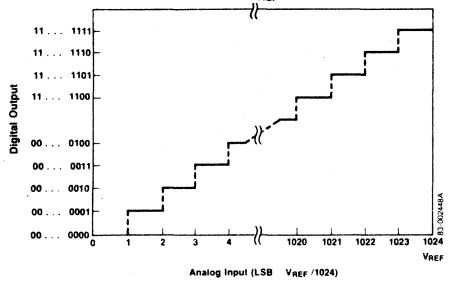
Read Mode (High Byte)



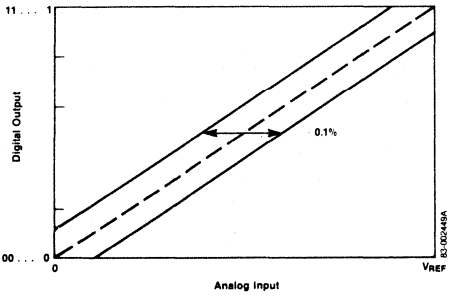
There is some uncertainty whether $\overline{EOC}$ is set or not, when data read operation is made simultaneously with the end of A/D conversion. Furthermore, the reading error occurs at this time, so in this case a dual read operation is recommended.

Operating Characteristics

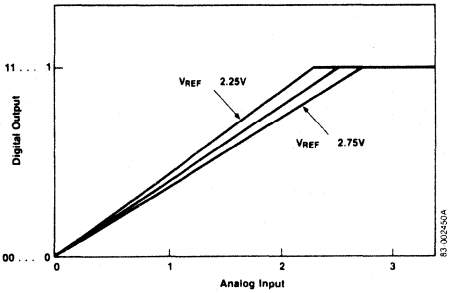
Full Scale vs V_{REF}



Total Unadjusted Error



Transfer Characteristics with Respect to V_{REF}



Addressing the Inputs

One of the four analog inputs is selected by initiating a write mode from the external controller with the control signals as follows: $\overline{CS}$ (pin 23) = "low," $\overline{RD}$ (pin 25) = "high," $\overline{WR}$ (pin 24) = "low," A1 (pin 27) and A0 (pin 26) = "low."

The analog input select data is presented to D0 (pin 22) and D1 (pin 21) and the desired channel (1 to 4) is selected. The conversion resolution mode is also selected during "write" mode by presenting a "high" for 10-bit mode or "low" for 8-bit mode, to D3 at pin 19.

Sequence

- ☐ Initiate "write" mode ($\overline{CS} = 0$, $\overline{RD} = 1$, $\overline{WR} = 0$, A1/A2 = 0).
- ☐ Present data for analog channel select to D0, D1.

	D0	D1
CH0 =	L	L
CH1 =	H	L
CH2 =	L	H
CH3 =	H	H

- ☐ Present conversion resolution data to D3.

10 BIT = H
8 BIT = L

During the write mode the only available function of the μPD7002 is data input from the controlling system. When the write function is terminated the A/D conversion process starts.

The Conversion Process

During the "write" mode the internal sequence controller is initialized and ready to take control of the conversion process on the rising edge of the write pulse. All conversion functions take place with the μPD7002 in the "not selected" mode with the control signals set at: $\overline{CS}$ = "low," $\overline{RD}$ and $\overline{WR}$ "high . . . A0" and A1 "don't care." In the A/D section the analog signal is input via the multiplexer and compared to V_{REF} at pin 8 (V_{REF} sets the maximum full-scale input signal which can be converted). At this point the internal sample and hold for auto zero function and full scale correction are accomplished.

The processed analog signal is then passed to the analog section where the integrating capacitor is charged for a given time period controlled by the clock. In this case the period is 8192 clock periods. The capacitor is then terminated to ground and the falling slope is measured by the number of clock cycles to the zero crossing point. The number of clock cycles from peak to zero (falling slope) is proportional to the value of V_{IN}. The integrator is then set up for the next conversion cycle.

The digital section converts the pulses from the analog section to 12-bit code and sends the converted code to the conversion data register where the data is latched and ready for "reading" by the controlling device. The data is then "read" in two bytes by addressing A0 and A1 while in the read mode. A1 = "low" A0 = "high" reads the high data byte (D0 to D7), and A1 = "high" A0 = "either" reads the low data byte (D7 to D4). During the low data byte read D0 to D3 are low and the data on D4 and D5 (bits 11 and 12) may not be accurate data.

The internal status can also be checked while in the read mode by setting A0 and A1 both "low."

Operation of Individual Sections

Sequence Controller (See Sequence Chart)

The Sequence Controller controls the internal sequence of A/D conversion and the operation of the three-state I/O buffer. It is initialized by the write mode operation (analog MPX address and 10-/8-bit choice). After the write mode operation, the Sequence Controller starts the A/D conversion, and outputs an $\overline{EOC}$ signal when the conversion is completed. There is no power-on-reset circuitry.

A/D Conversion Block

In the A/D section, an analog signal is input through the MPX and is compared to V_{REF}, after which it is converted to a digital output signal. Full scale analog input is equal to V_{REF}. GND as an analog input is equal to zero scale. A/D conversion time depends on both analog input voltage and conversion mode (10/8 bit).

Three-State I/O Port Section

The three-state I/O port section is controlled by the Sequence Controller. It accepts the MPX address input and conversion mode input (10-/8-bit choice). The three-state I/O port section outputs the internal status and conversion data high/low bytes.

Conversion Data Latch

After the end of conversion, the A/D section outputs new data to the Data Latch. The output of the Data Latch is connected to the three-state I/O ports, and the data can be read at any time. When Data Read occurs simultaneously with an internal data transfer, a read error occurs. Therefore, two read operations should be made, unless Data Read occurs after the end of conversion.

Status Latch

The status latch stores the status data internal to the chip, and the internal operation state can be referenced by the status data. Status includes the following:

$\overline{BUSY}$, $\overline{EOC}$: Internal sequence state of μPD7002. Write mode operation sets $\overline{BUSY}$, and this is reset at the end of conversion. $\overline{EOC}$ is set at the end of conversion, and High Byte Read Operation resets $\overline{EOC}$.

MSB, 2nd; 10-/8-Bit Flag MPX

The data stored in the conversion Data Latch when the status reading operation is made can be output. Therefore, the data is refreshed at the end of conversion.

Access to the μPD7002 from the CPU can be made by both interrupt and polling methods. In the interrupt method use $\overline{EOC}$ as an interrupt signal. In the polling method, use $\overline{EOC}$ and $\overline{BUSY}$ in Status Byte.

After the A/D conversion, the data in the conversion Data Latch does not change, and can be read repeatedly. Therefore, fundamental instructions like Load, Store, Move, etc. can be used to access data (by placing the address of the μPD7002 in memory area). Note that the access time (t_{RD}) and the data setup time (t_{DW}) of the μPD7002 are longer than that of the 8080 and 8085. The following program example shows the accessing of the μPD7002 by polling method in an 8080-based system.

MPX Channel Address Functions

MPX Address Bit	Analog Input Channel			
	CH0	CH1	CH2	CH3
D_1	L	L	H	H
D_0	L	H	L	H

Control Terminal Functions

Control Terminals					Mode	Internal Function	Data I/O Terminals
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_7			
H	X	X	X	X	Not selected		High impedance
L	H	H	X	X	Not selected	—	
L	H	L	L	L	Write mode	Data latch A/D start	Input status, D_1, D_0 = MPX address D_3 = 8-bit/10-bit conversion designation. Note 1. D_7 = Flag input.
L	H	L	L	H	Not selected	—	High impedance
L	H	L	H	L	Not selected	—	
L	H	L	H	H	Test mode	Test status	Input status, Note 2
L	L	H	L	L	Read mode	Internal status	$D_7 = \overline{EOC}$, D_6 = BUSY, D_5 = MSB, D_4 = 2nd MSB, D_3 = 8/10, D_2 = Flag Output, D_1 = MPX, D_0 = MPX
L	L	H	L	H	Read mode	High data byte	D_7–D_0 = MSB – 8th bit
L	L	H	H	L	Read mode	Low data byte	D_7–D_0 = 9th – 10th bit
L	L	H	H	H	Read mode	Low data byte	D_3–D_0 = L

Notes: 1. Designation of number of conversion bits: 8 bit = L; 10 bit = H.
2. Test Mode: used for inspecting the device. The data input-output terminals assume an input state and are connected to the A/D counter. Therefore, the A/D conversion data read out after this is meaningless.

Bit Function

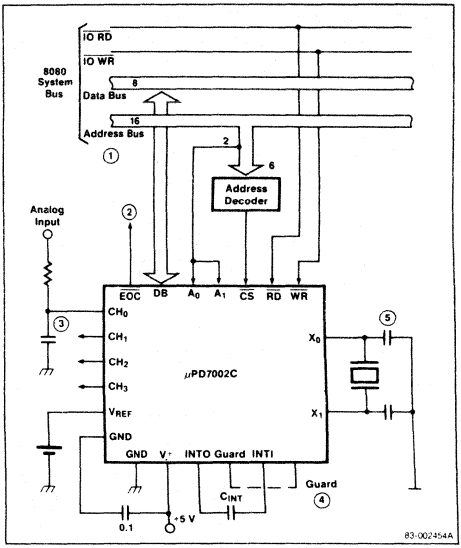
		Write Mode	Read Mode				
		Function	Status Output	High Byte Output		Low Byte Output	
Bit	I/O			10-Bit Note 2	8-Bit	10-Bit Note 2	8-Bit
D7	Output		EOC	MSB	MSB	9th	Note 3
D6	Output		Busy	2nd	2nd	LSB	Note 3
D5	Output		MSB Note 1	3rd	3rd	Q_{11}	Note 3
D4	Output		2nd Bit Note 1	4th	4th	Q_{12}	Note 3
D3	I/O	10/8-Bit	10/8-Bit Note 1	5th	5th	Low	Low
D2	I/O	Flag input	Flag Output Note 1	6th	6th	Low	Low
D1	I/O	MPX Address	MPX Note 1	7th	7th	Low	Low
D0	I/O	MPX Address	MPX Note 1	8th	8th	Low	Low

Notes: 1. Previous conversion data.
2. In 10-bit mode, the μPD7002 operates as a 12-bit converter. Therefore, 11th and 12th bit data appear at Q_{11} and Q_{12}, and the output of Q_{11} and Q_{12} varies with analog input; however, the data contain internal noise and are meaningless.
3. Not to be determined.

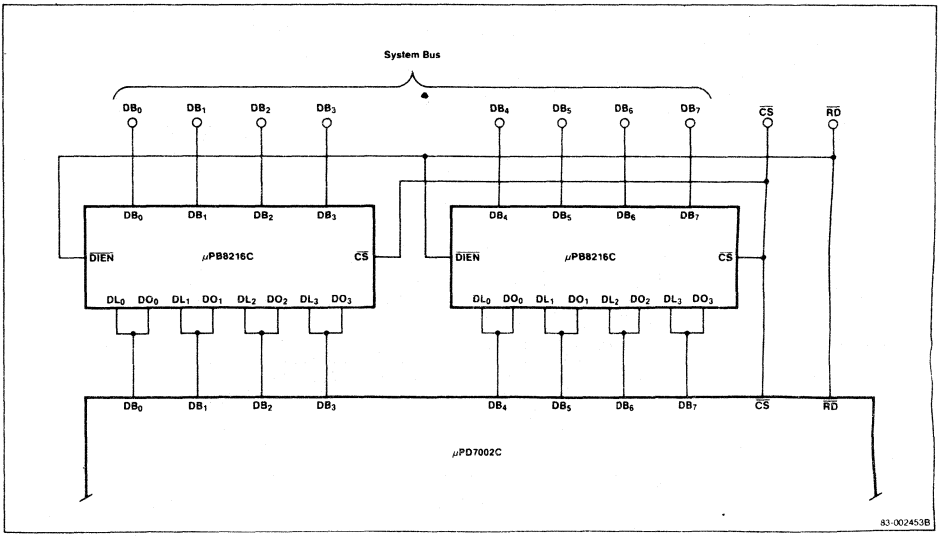
Typical Applications

1. The high level input voltage of the μPD7002C is 2.2 V. In a minimum component system configuration, tying 50 kΩ resistors to DB_0-DB_7, A_0, A_1, $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ is recommended. The fan-out of DB_0-DB_7 is 1 TTL level. In larger systems, use bus drivers as shown here.
2. Use $\overline{EOC}$ as an interrupt signal if you have an interrupt-driven system.
3. Use a 100 Hz low pass filter to decrease the conversion error. Using the diode protection circuit shown here is effective protection against high voltage surges.
4. The μPD7002 uses the integration technique for A/D conversion, and it operates at a very low current level. The external integrating capacitor (C_{INT}) is directly connected to the internal integrator. Using the guard pattern as shown below makes the operation less sensitive to leakage current.
5. Capacitors are tied to the X and X_0 pins to stabilize the oscillation, use a ceramic capacitor about 50 pF. About 50 ms is required for stable oscillation after initial power-on. Therefore, the first Write Mode Operation should occur after this interval.

Typical Microprocessor Interface

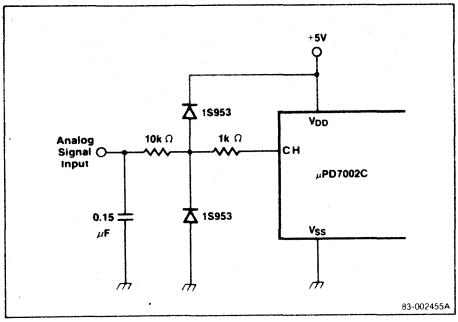


Use of Bus Drivers

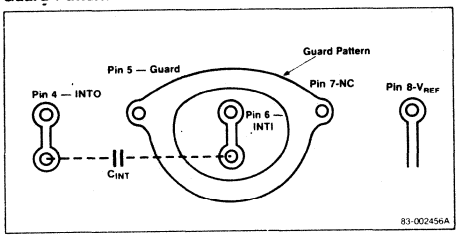


Typical Applications (Cont.)

Diode Protection Circuit



Guard Pattern

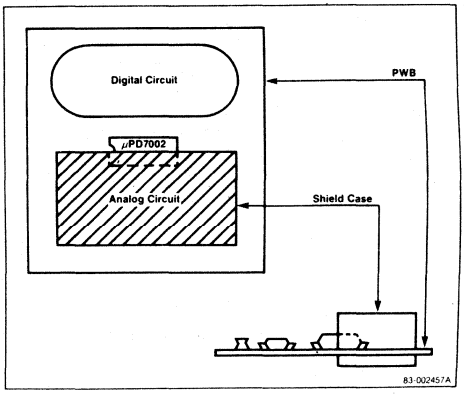


Noise Reduction

The μPD7002 is an integrating A/D converter; however, it operates at a relatively high speed and the normal mode noise rejection cannot be expected. Observance of the following points will minimize noise induction to the input of the analog circuit.

- ☐ Use lower impedance in GND connection
- ☐ Place the bypass capacitors for supply voltage and V_{REF} and analog input close to the μPD7002 (one point GND is also effective)
- ☐ Isolate analog circuitry from digital circuitry:
  - — Component layout
  - — GND wire layout
  - — Shielding of analog circuitry (pin configuration of the μPD7002 is suitable for the layout shown in the next figure)

Shield for Analog Circuitry



APPLICATION HINTS

1. EXTERNAL CLOCK

IF EXTERNAL CLOCK IS USED XI (PIN 2) SHOULD BE USED FOR CLOCK INPUT. XO (PIN 1) SHOULD BE LEFT OPEN.

2. D 2 FLAG INPUT/OUTPUT

D 2 FLAG INPUT DURING WRITE MODE CAN FREELY BE SET OR RESET WITHOUT ANY INFLUENCE TO THE A/D CONVERTER ITSELF. D 2 FLAG OUTPUT DURING STATUS READ WILL HAVE THE CONTENTS AS PROGRAMMED DURING D 2 INPUT.

3. RESOLUTION

INTERNAL RESOLUTION IS 12 BIT BUT 11TH AND 12TH BIT DATA CONTAINS THE INTERNAL NOISE ONLY, ALLTHOUGH THEY VARY WITH ANALOG INPUT. TO INTRODUCE THE 7002 AS A 10 BIT A/D CONVERTER SHOULD BE BETTER AND WILL STOP CONFUSION ON THIS MATTER.

4. GUARD PINS

TO MAKE THE 7002 LESS SENSITIVE AGAINST LEAKAGE CURRENT THE GUARD PIN (PIN 5 AND 7) SHOULD BE USED IN THE WAY SHOWN ON THE PAGE 20.

Description

The μPD7003 is a high speed, high performance, low power, 8-bit analog-to-digital Converter designed to be easily interfaced to the 8080 and 8086, 8- and 16-bit microprocessors. Using the parallel conversion technique, the μPD7003 features a conversion speed of 4 μs and eliminates the need of sample and hold circuits in most applications. The μPD7003 is also capable of running under DMA control using a DMA controller such as the μPD8257. Available in a 24-pin ceramic/plastic DIP, the μPD7003 is the ideal converter for high speed 8-bit designs.

Features

- ☐ High speed conversion (250 k samples/sec. max.)
- ☐ Input consists of 255/1 matched autozeroed comparators
- ☐ No missing codes over temperature range
- ☐ Linearity ±1.25 LSB max.
- ☐ Three-state outputs
- ☐ Overrange output
- ☐ Operates from single +5 V supply
- ☐ Low power consumption (50 mW)

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7003C	Plastic DIP	−20 °C to +70 °C
μPD7003D	Ceramic DIP	−20 °C to +80 °C

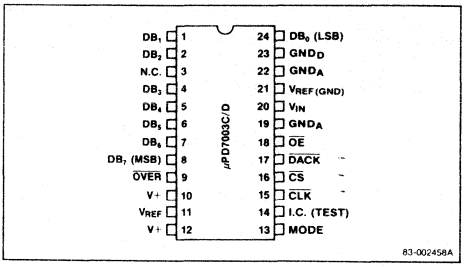
Absolute Maximum Ratings

T_A = 25 °C

Operating Temperature, C Package	−20 to +70 °C
Operating Temperature, D Package	−20 to +70 °C
Storage Temperature	−65 to +125 °C
All Input Voltages	−0.3 to V+ +0.3 V
Power Supply	−0.3 to +7 V
Power Dissipation	300 mW
Analog GND Voltage	±0.3 V

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Pin Identification

Pin	Name	Function
1	DB_1	7th bit output
2	DB_2	6th bit output
3	NC	Non connection
4	DB_3	5th bit output
5	DB_4	4th bit output
6	DB_5	3th bit output
7	DB_6	2th bit output
8	DB_7	MSB output
9	$\overline{OVER}$	Overrange output
10	V+	Power supply (+5 V)
11	V_{REF}	Reference voltage input (positive)
12	V+	Power supply (+5 V)
13	MODE	MODE control (note 1)
14	TEST	Low: Device test (used for inspecting the device) High: Conversion
15	$\overline{CLK}$	Low: Previous data output High: Quantizing
16	$\overline{CS}$	Chip select
17	$\overline{DACK}$	DMA Acknowledge
18	$\overline{OE}$	Low: Data output High: High impedance
19	AGND	Analog ground
20	V_{IN}	Voltage input
21	$V_{REF(GND)}$	GND for V_{REF}
22	AGND	Analog ground
23	GND	Digital ground
24	DB_0 (LSB)	LSB

Pin Identification (Cont.)

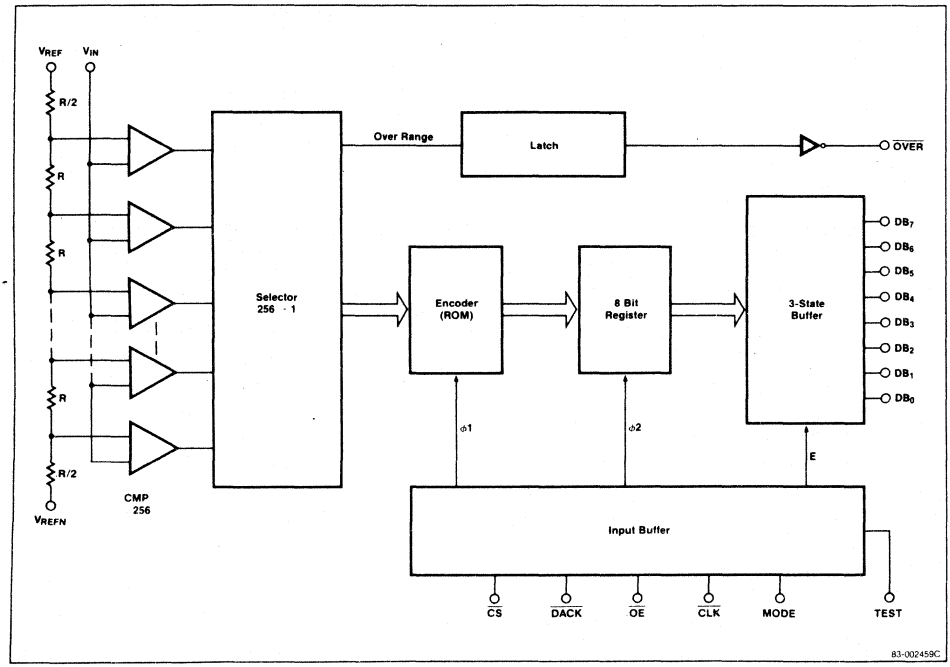
Pin	Name	Function
19	GND_A	Analog ground
20	V_{SIN}	Analog input
21	V_{REFN}	Reference voltage input (negative) (Note 2)
22	GND_A	Analog ground
23	GND_D	Digital Ground
24	DB0	LSB output

Notes: 1.

Inputs		8-Bit Register
Mode	$\overline{OE}$	
1	1	Data refreshed with every $\overline{CONV}$ ↓
	0	
0	1	
	0	No change

2. Tie to the analog ground unless external zero adjustment required.

Block Diagram



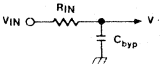
DC Characteristics

$T_A = +25°C$, $V+ = V_{REF} = 5.0 \pm 0.25$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Current	I_{CC}		6.0	18.0	mA	$t_{CY} = 4.0\ \mu s$, $t_{WLC} = 2.0\ \mu s$ Note 1
High Level Output Voltage	V_{OH}	2.8			V	$I_O = -2.0$ mA
Low Level Output Voltage	V_{OL}			0.4	V	$I_O = -1.0$ mA
Digital Input Leakage Current	I_{ILK}		1	10	μA	$0\ V \leq V_{IN} \leq V+$
Digital Output Leakage Current	I_{OLK}		1	10	μA	$0\ V \leq V_O \leq V+$
Reference Input Current	I_{REF}	1.19	1.79	3.57	mA	$\overline{CLK}$ = H or L Note 1
Analog Input Resistance	R_{IN}	1	35		kΩ	$V_{EN} = 2.5$ V, $t_{CY} = 4\ \mu s$, $t_{WLC} = 2\ \mu s$ Note 2
Reference Input Capacitance	C_{REF}		100		pF	$f_{clk} = 1$ MHz; unmeasured pins returned to Ground
Analog Input Capacitance	C_{IN}		100		pF	$f_{clk} = 1$ MHz; unmeasured pins returned to Ground
Power Dissipation	P_D			50	mW	$t_{CY} = 4.0\ \mu s$, $t_{WLC} = 2.0\ \mu s$

Notes: 1. This means DC current. Tie the bypass capacitors (electrolytic capacitor ≥ 10 μF, ceramic capacitor ≈ 0.01 μF) to V+ and V_{REF} pins, in order to absorb rush current (≈ 10 mA).

2. DC input equivalent circuit is shown below.



Tie the bypass capacitor (> 0.01 μF) to the analog input pin. 3 mA peak current flows into this pin.

AC Characteristics

$T_A = 25 \pm 2°C$; $V+ = 5.0$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Delay Time	t_{DEO}		100	350	ns	$\overline{OE}$ ↓ → DO
	t_{DCO}		150	450	ns	$\overline{CONV}$ ↓ → DO
	t_{DSO}		100	350	ns	$\overline{CS}$ ↓ → DO
	t_{DCOVR}		100	350	ns	$\overline{CONV}$ ↑ → $\overline{OVER}$
Delay Time to Floating	t_{FEO}		70	200	ns	$\overline{OE}$ ↑ → DO
	t_{FSO}		150	450	ns	$\overline{CS}$ ↑ → DO

Conversion Characteristics

$T_A = 25 \pm 2°C$; $V+ = V_{REF} = 5.0$ V;
$t_{CY} = 4.0\ \mu s$; $t_{WLC} = 2.0\ \mu s$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution	RES	8	8	8	Bits	−20°C to +80°C
Nonlinearity	NL			±1.25	LSB	
Full Scale Error				±1.00	LSB	
Full Scale Error Temperature Coefficient			20		ppm/°C	
Zero Scale Error		−0.75		+0.75	LSB	
Zero Scale Error Temperature Coefficient			20		ppm/°C	

Note: μPD7003C: $T_A = 0°C$ to $+70°C$.

Recommended Operating Conditions

T_A = 0°C to 70°C: μPD7003C,
T_A = −20°C to +80°C: μPD7003D

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	4.75	5.0	5.25	V	
Reference Input Voltage	V_{REF}	4.0	V+	V+	V	
Analog Input Voltage	V_{IN}	−0.1		V+ +0.1	V	
High Level Logic Input	V_{IH}	2.4		V+	V	
Low Level Logic Input	V_{IL}	−0.1		0.8	V	
Sampling Rate		10		250k	times/s	
Conversion Cycle Time	t_{CY}	4.0		100	μs	
$\overline{CONV}$ High Level Width	t_{WHC}	2.0			μs	
$\overline{CONV}$ Low Level Width	t_{WLC}	2.0			μs	
$\overline{CONV}$ Setup Time	t_{SCE}	0		Note 1	ns	$\overline{CONV}$ ↓ → $\overline{OE}$ ↓
$\overline{CS}$ Setup Time	t_{SSE}	100			ns	$\overline{CS}$ ↓ → $\overline{OE}$ ↓
$\overline{CS}$ Hold Time	t_{HES}	0			ns	$\overline{OE}$ ↑ → $\overline{CS}$ ↑
$\overline{OE}$ Setup Time	t_{SEC}	600			ns	$\overline{OE}$ ↓ → $\overline{CONV}$ ↓
$\overline{OE}$ Hold Time	t_{HCE}	400			ns	$\overline{CONV}$ ↑ → $\overline{OE}$ ↓
$\overline{OE}$ Low Level Width	t_{WLE}	400		Note 2	ns	
Digital Input Rise and Fall Time	t_r, t_f			50	ns	

Notes: 1. t_{SCE} (ns) ≤ t_{CY} (ns) − t_{WLE} (ns) − 100 (ns).
2. t_{WLE} (ns) ≤ t_{CY} (ns) − t_{SCE} (ns) − 100 (ns).

Converter Operation

Referring to the block diagram, the reference voltage is set externally to some desired level which references the individual internal components such that V_{REF} is divided equally by 256 resistors in a ladder/divider configuration. The applied voltage to V_{IN} is then compared to the reference level and the individual samples are sent to the selector section where the individual signals are multiplexed to form an address data word. The data word is then further encoded to form the final 8-bit data byte by the encoder ROM, and stored in the 8-bit register until the Output Enable Command. Then the data is sent to the data bus via a three-state buffer.

Mode Select

There are two modes of operation for the μPD7003. Figure 1 shows the timing diagram for mode "0" where the converter is operating in continuous output mode. The analog input is sampled when the clock is in the "low" state. When the clock is in the "high" state the conversion from analog-to-digital takes place and the resultant data is output on the next falling edge of the clock pulse and the cycle is repeated.

The second mode (Mode 1) is shown in figure 2. In this mode of operation, one conversion takes place while the clock is in the "low" state and the resultant data is held as long as output enable and Chip Select ($\overline{CS}$) or DMA Acknowledge ($\overline{DACK}$) are "low." Data refresh is inhibited until $\overline{CS}$ and $\overline{DACK}$ are recycled.

MODE = "HIGH"

Data is refreshed on the falling edge of $\overline{CLK}$, loaded during the "low" clock state, and converted and output during the "high" clock state.

MODE = "LOW"

Data is loaded and converted when Output Enable is "low" and refreshed only when $\overline{OE}$ makes the transition from high to low again.

Note that in either case data will only be accepted and output when $\overline{OE}$ and $\overline{CS}$ or $\overline{DACK}$ are active ("low"). Output enable should not be changed during the intervals shown in figure 3. The timing for output enable change versus clock transition is 600 ns before and 500 ns after the rising or falling edge of $\overline{CLK}$ any attempt to change $\overline{OE}$ during these periods will be inhibited.

Timing Waveforms

Figure 1. (MODE;0)

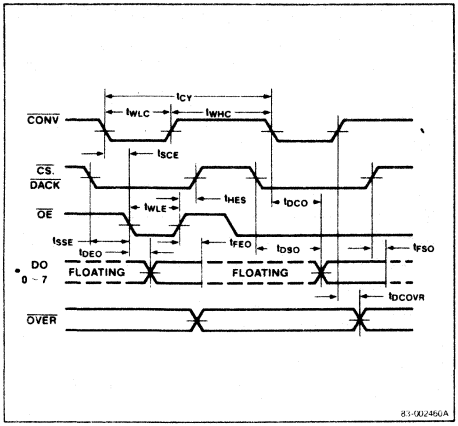


Figure 2. (MODE;1)

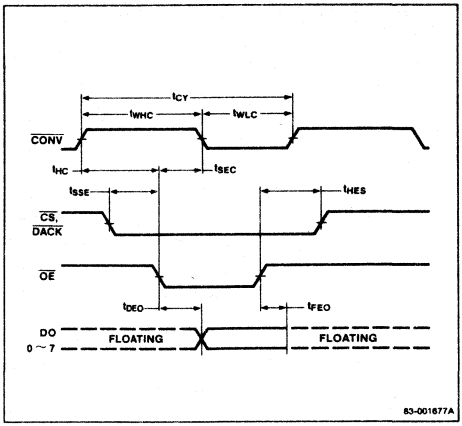
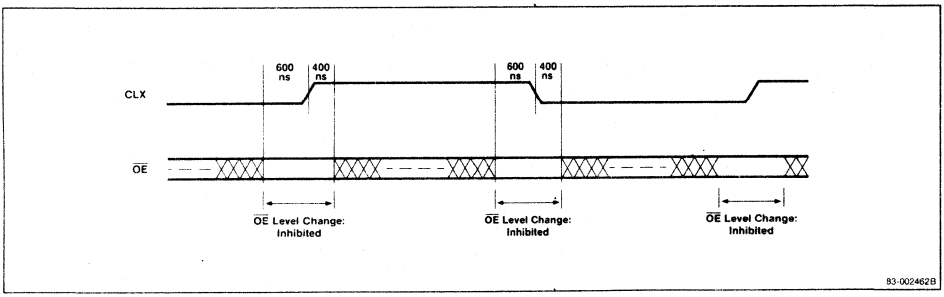
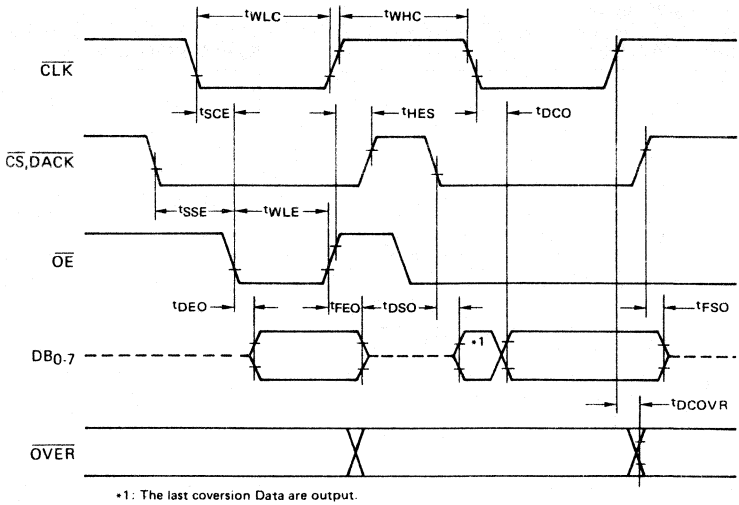


Figure 3. Timing Chart



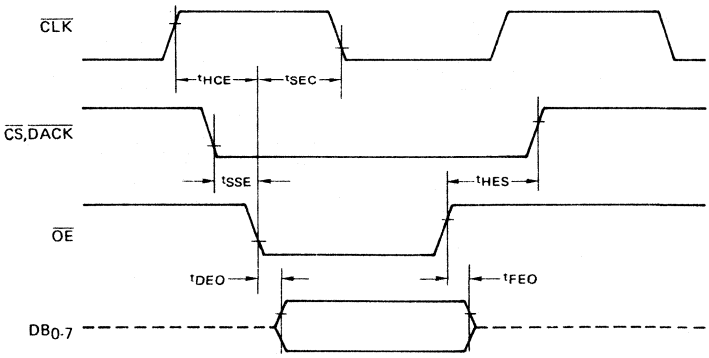
TIMING DIAGRAMS

1. CONTINUOUS OUTPUT MODE



*1: The last coversion Data are output.

2. LATCH OUTPUT MODE



OPERATION OF INTERNAL CIRCUIT BLOCK

1. COMPARATOR

Reference voltage (V_{REF}) is divided by 256 resistors, and 256 comparators simultaneously compare analog input voltage (V_{IN}) with the divided voltages.

2. SELECTOR, ENCODER

Selector accepts the outputs of comparators, and detects the position of comparator which corresponds to analog input voltage.

The encoder generates an 8 bit code by translating the output data from selector.

When the analog input voltage (V_{IN}) is higher than the reference voltage (V_{REF}), the selector generates an over range signal ($\overline{OVER}$).

3. 8-BIT LATCH

This register temporally stores 8-Bit data from encoder.

4. LOGIC CONTROL

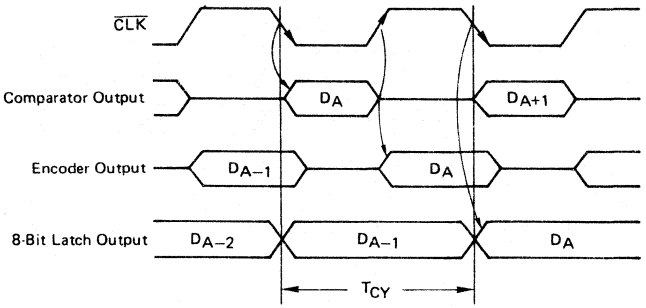
This circuit block generates internal control signals according to external control signals.

OPERATION MODES According to the different conversion output, two modes of operation are available.

1. CONTINUOUS OUTPUT MODE (MODE = H)

The actual conversion time of μPD7003 is shortened by using pipeline processing mode.

INTERNAL TIMING

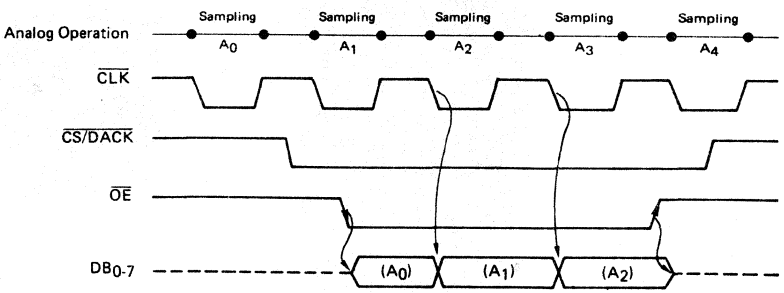


The pipeline processing consists of 3 steps:

- Comparing by comparators,
- Generating 8-Bit data in selector and encoder,
- Holding conversion data in 8-Bit latch.

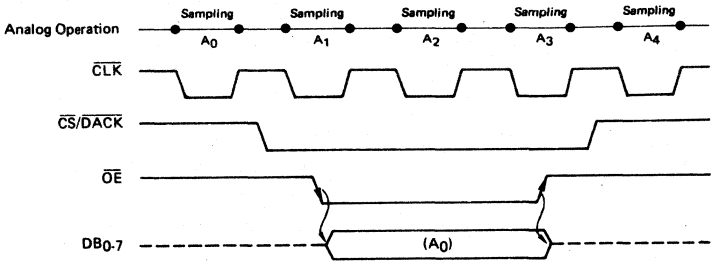
Analog input signals are sampled at the low level interval of $\overline{CLK}$. The conversion data are output at the subsequent falling edge of $\overline{CLK}$.

CONTINUOUS OUTPUT MODE TIMING

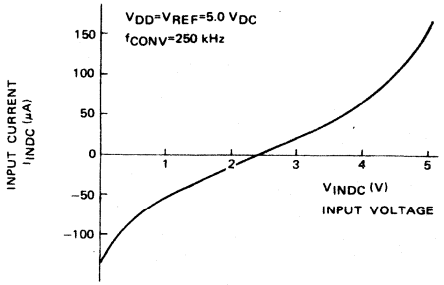


2. LATCH OUTPUT MODE (MODE = L)

In this mode, μPD7003 operates the same A/D conversion operation as continuous output mode, but with an additional 8-Bit latch operation. In latch output mode, updating of 8-Bit latch data is inhibited at the low level interval of $\overline{OE}$, and holding the last latched data.

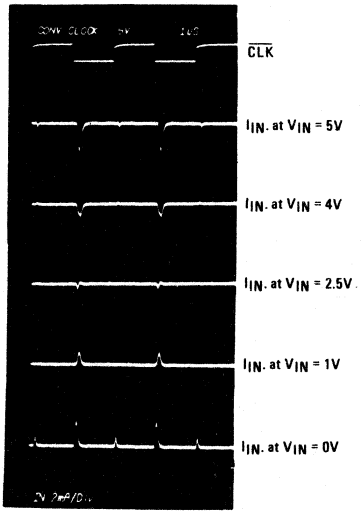


INPUT CHARACTERISTICS



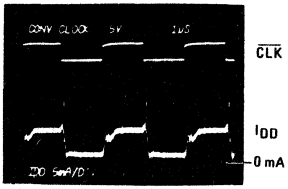
INPUT CURRENT WAVEFORMS

I_{IN}: (V_{DD} = V_{REF} = 5.0V, f_{CLK} = 250 kHz)



POWER SUPPLY CURRENT WAVEFORMS

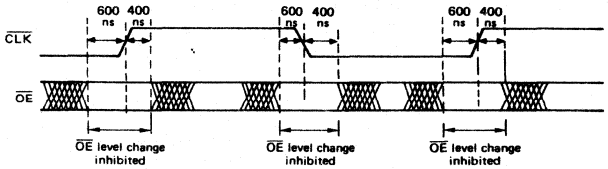
I_{DD} (V_{DD} = V_{REF} = 5.0V, f_{CONV} = 250 kHz)



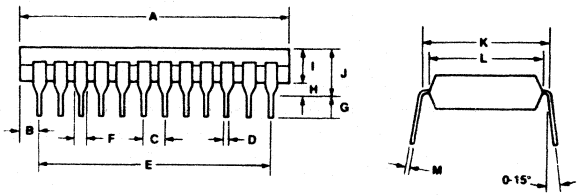
APPLICATION HINTS

Note 1: Data of A_1 and A_2 are not held.

Note 2: Please do not change the level of $\overline{OE}$ signal during the intervals shown below.

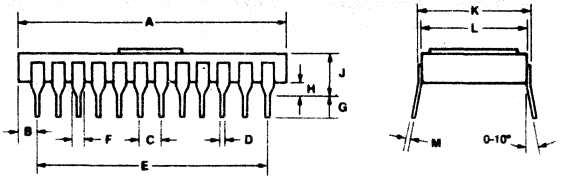


PACKAGE OUTLINE
μPD7003C
(PLASTIC)



ITEM	MILLIMETERS	INCHES
A	33 max	1.3 max
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 min	0.1 min
H	0.5 min	0.02 min
I	5.22 max	0.205 max
J	5.72 max	0.225 max
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

PACKAGE OUTLINE
μPD7003D
(CERAMIC)



ITEM	MILLIMETERS	INCHES
A	30.78 max	1.21 max
B	1.53 max	0.06 max
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 min	0.04 min
G	3.2 min	0.13 min
H	1.02 min	0.04 min
I	3.23 max	0.13 max
J	4.25 max	0.17 max
K	15.24 typ	0.60 typ
L	14.93 typ	0.59 typ
M	0.25 ± 0.05	0.010 ± 0.002

Description

The μPD7004 is a 10-bit monolithic CMOS analog-to-digital converter using the Successive Approximation Register (SAR) technique. The μPD7004 incorporates an 8-channel multiplexed analog input and full microprocessor interface to achieve a high degree of versatility. The designer has a choice of either serial or parallel output and interface to 8080 type microprocessors or advanced signal processors like the μPD7720.

Features

- ☐ 8-channel multiplexed analog input
- ☐ Serial or parallel interface
- ☐ 10-bit resolution
- ☐ Linearity: 1 LSB max. (T_A = 25°C)
- ☐ Conversion time: 100 μs (f_{clk} = 1 MHz)
- ☐ Input voltage range 0 to V+
- ☐ Temperature range from −40 to +85°C
- ☐ Operates from single +5 volt supply

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7004C	Plastic DIP	−40°C to +85°C

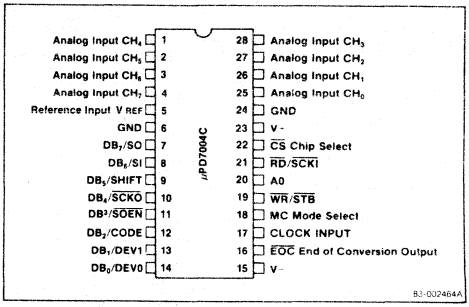
Absolute Maximum Ratings

T_A = 25°C

Supply Voltage, V_{DD}	−0.3 to +7.0 V
Input Voltage, V_I	−0.3 to V+ +0.3 V
Reference Voltage, V_{REF}	−0.3 to V+ +0.3 V
Operating Temperature, T_{OPT}	−40 to +85°C
Storage Temperature, T_{OPT}	−65 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Conversion Characteristics

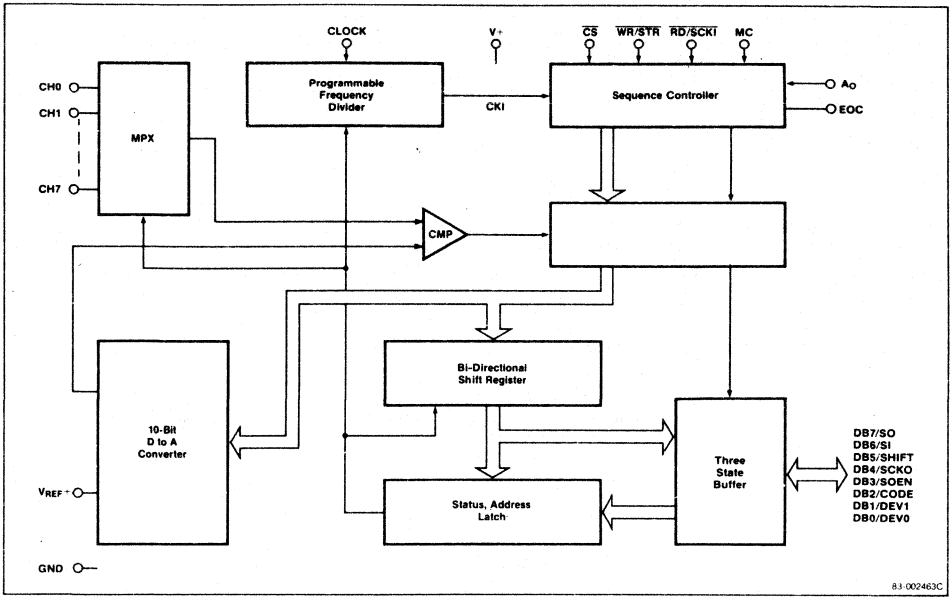
T_A = 25°C, V+ = V_{REF} = 4.5 to 5.5 V,
f_{clk} = 1 MHz

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		10	10	10	Bit	−40 to +85°C
Nonlinearity	NL			±1.0	LSB	
Zero Scale Error				±0.5	LSB	
Zero Scale Temperature Coefficient			2		ppm/°C	−40 to +85°C
Full Scale Error		−0.5		0.5	LSB	
Full Scale Temperature Coefficient			2		ppm/°C	−40 to +85°C
Nonlinearity	NL			±2	LSB	−40 to +85°C ($T = T_{OPT}$)

Pin Identification

		Parallel Mode		Serial Mode	
Pin	Symbol	Direction	Function	Direction	Function
1	CH4		Analog input CH4		
2	CH5		Analog input CH5		
3	CH6		Analog input CH6		
4	CH7		Analog input CH7		
5	V^+_{REF}		Positive reference input		
6	GND		Ground		
7	DB7/SO	O	Data bus (MSB)	O	Serial output
8	DB6/SI	O	Data bus (2nd)	I	Serial input
9	DB5/SHIFT	O	Data bus (3rd)	I	LSB/MSB 1st select
10	DB4/$\overline{SCKO}$	O	Data bus (4th)	I/O	Serial clock output
11	DB3/$\overline{SOEN}$	O	Data bus (5th)	I/O	Serial output enable
12	DB2/CODE	I/O	Data bus (6th)	I	Code select
13	DB1/DEV1	I/O	Data bus (7th	I	Frequency divide ratio set
14	DB0/DEV0	I/O	Data bus (LSB)	I	Frequency divide ratio set
15	V+		Power supply		
16	$\overline{EOC}$	O	End of conversion (active low)		
17	CLOCK	I	Clock input		
18	MC	I	MODE select (H = Parallel, L = Serial)		
19	$\overline{WR}/\overline{STB}$	I	Write input	I	Strobe input
20	A0	I	Address input	I	Internal/external shift clock
21	$\overline{RD}/\overline{SCKI}$	I	Read input	I	Serial clock input
22	$\overline{CS}$	I	Chip select		
23	V+		Power supply		
24	GND		Ground		
25	CH0		Analog input CH0		
26	CH1		Analog input CH1		
27	CH2		Analog input CH2		
28	CH3		Analog input CH3		

Block Diagram



AC Characteristics

$T_A = -40°C$ to $+85°C$, $V+ = V_{REF} = 5\ V \pm 0.5\ V$, $f_{CKI} = 1\ MHz$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Delay Time	t_{RD}			250	ns	$\overline{RD}$ ↓ → DB (parallel mode)
	t_{DKO}			250	ns	$\overline{SCKI}$ ↓, $\overline{SCKO}$ ↓ → SO (serial mode)
Output Floating Delay Time	t_{DF}			150	ns	$\overline{RD}$ ↑ → DB floating (parallel mode)
	t_{FCSO}			150	ns	$\overline{CS}$ ↑ → SO floating (serial mode 1)
Serial Clock Output Delay Time	t_{SKS}	40		200	ns	$\overline{SCKO}$ ↑ → $\overline{SOEN}$ ↓ (serial mode 2)
Serial Output Enable Delay Time	t_{HKS}	0		200	ns	$\overline{SCKO}$ ↓ → $\overline{SOEN}$ ↑ (serial mode 2)
Serial Clock Output Cycle	t_{CYK}		$1/f_{clk}$		ns	(Serial mode 2)
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	(Serial mode 2)
Low Level Serial Clock Pulse Width	t_{WLK}	400			ns	(Serial mode 2)
Serial Clock Rise Time	t_{RSC}		20		ns	(Serial mode 2)
Serial Clock Fall Time	t_{FSC}		20		ns	(Serial mode 2)

DC Characteristics

$T_A = -40°C$ to $+85°C$, $V_{REF} = 5\ V \pm 0.5\ V$, $f_{clk} = 1\ MHz$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
High Level Output Voltage	V_{OH}	3.5			V	$I_O = -1.6\ mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_O = 1.6\ mA$
Digital Input Leakage Current	I_{ILK}	−10		10	μA	V_{IN} = GND
High-Z Output Leakage Current	I_{OLK}	−10		10	μA	V_O = GND
Analog Input Resistance	R_{IN}		1000		MΩ	V_{IN} = GND
Equivalent Analog Input Resistance	R_{IN}		10		kΩ	Analog input impedance is equivalent to that of the series circuit of R_I and C_I
	C_{IN}		100		pF	
Reference Input Resistance	R_{REF}	5		50	kΩ	
Power Dissipation	P_D		5	15	mW	

Recommended Operating Conditions

$T_A = -20°C$ to $+80°C$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V+	4.5	5.0	5.5	V	
Reference Voltage	V_{REF}	4.0		V_{DD}	V	
Analog Input Voltage	V_{IN}	0.0		V_{REF}	V	
High Level Input Voltage	V_{IH}	2.4			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Clock Frequency	f_{clk}	0.4		8.8	MHz	
Internal Clock Frequency	f_{clki}	0.4	1.0	1.1	MHz	$f_{clki} = f_{clk} \times$ Divide Ratio
Parallel Mode (MC = High)						
Address Setup Time	t_{AW}	50			ns	$\overline{CS}\downarrow$, AO → $\overline{WR}\downarrow$
	t_{AR}	50			ns	$\overline{CS}\downarrow$, AO → $\overline{RD}\downarrow$
Address Hold Time	t_{WA}	50			ns	$\overline{WR}\uparrow$ → $\overline{CS}\uparrow$ AO
	t_{RA}	50			ns	$\overline{RD}\uparrow$ → $\overline{CS}\uparrow$, AO
$\overline{WR}$ Pulse Width	t_{WW}	400			ns	
$\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time	t_{DW}	300			ns	DB → $\overline{WR}\uparrow$
Data Hold Time	t_{WD}	100			ns	$\overline{WR}\uparrow$ → DB
Serial Mode 1 (MC = Low, AO = Low; External Serial Clock)						
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}\downarrow$ → $\overline{CS}\downarrow$
$\overline{CS}$ Setup Time	t_{SCSK}	1			μs	$\overline{CS}\downarrow$ → $\overline{SCKI}\downarrow$
Serial Input Setup Time	t_{SIK}	150			ns	SI → $\overline{SCKI}\uparrow$
Serial Input Hold Time	t_{HKI}	100			ns	$\overline{SCKI}\uparrow$ → SI
Low Level Serial Clock Pulse Width	t_{WLK}	400			ns	
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	
Strobe Pulse Width	t_{WLST}	200			ns	
Strobe Hold Time	t_{HKST}	200			ns	$\overline{SCK}\uparrow$ → $\overline{STB}\uparrow$
Chip Select Hold Time	t_{HKCS}	100			ns	$\overline{SCK}\uparrow$ → $\overline{CS}\uparrow$

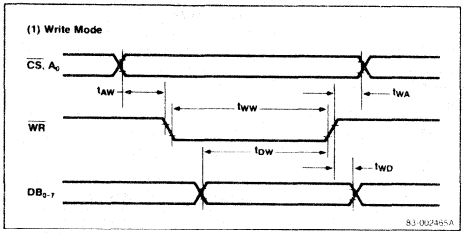
Addressing the Inputs

One of eight analog inputs can be selected with the μPD7004 in the "write" mode and A0 at pin 20 set "low." The "write" mode is selected by setting the Chip Select ($\overline{CS}$) at pin 22, and Write ($\overline{WR}$) at pin 19, "low" or 0. The multiplex channel select is accomplished by presenting a 3-bit binary code to DB0 to DB2 at pins 14, 13, and 12 where 000 = channel 0 and 111 = channel 7.

Referring to figure 1, the sequence is:

- ☐ Chip Select ($\overline{CS}$) and A0 set "low."
- ☐ Write ($\overline{WR}$) set "low." (Read ($\overline{RD}$) is left "high.")
- ☐ Analog input channel selected by presenting a 3-bit binary code on pins 14, 13, 12 (D0 to D2).
- ☐ The address is latched and the desired input channel is now selected.

Figure 1. Write Mode Timing Diagram



Initializing the Converter

The μPD7004 gives the designer a choice of the type of data output format, either a 2's complement or binary, and the speed of operation by providing a programmable frequency divider. These options may be selected by the controlling system at any time by the "initialize" mode.

The "initialize mode" is set with $\overline{CS}$ and $\overline{WR}$ both "low." $\overline{RD}$ and A0 are set "high." Code select is accomplished by presenting either a "high" for 2's complement or "low" for binary output at DB2 (pin 12). The divide ratio of 1/1 to 1/8 is set by presenting a 2-bit code to DB0 (pin 14) and DB1 (pin 13).

Ratio	DB0	DB1
1/1	L	L
1/2	H	L
1/4	L	H
1/8	H	H

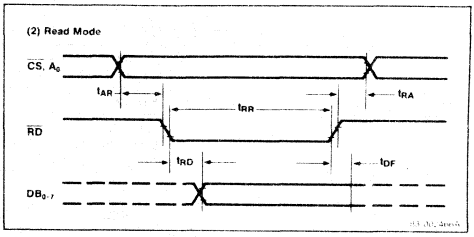
Data Output

Data can be read in 2 bytes from the data output at pins 7 through 14 (DB7 to DB0). To read the high byte, $\overline{CS}$ and $\overline{RD}$ are both "low." To read the low byte, A0 is set Low and data bit 9 and 10 are present at DB7 and DB6 respectively. During the low data byte read DB0 through DB5 are "low."

Referring to figure 2, the sequence is:

- ☐ Chip Select ($\overline{CS}$) "low" and A0 (pin 20) "high"
- ☐ Read ($\overline{RD}$) set "low" and Write ($\overline{WR}$) set "high"
- ☐ Output high byte (MSB to 8th bit)
- ☐ A0 set "low"
- ☐ Output low byte (9th bit and LSB)

Figure 2. Data Output Timing Diagram



The Conversion Sequence

The μPD7004C uses the Successive Approximation Register (SAR) technique to convert analog voltage levels to 10-bit digital code in either 2's complement or binary format. Regardless of the type of data output (either serial or parallel), the conversion process is the same.

Once the clock frequency and the output data format have been set, and the analog input selected, the conversion process begins with the analog level compared to the existing level from an internal 10-bit digital to analog converter. The D/A output level is proportional to the existing code output from the Successive Approximation Register which is proportional to the input level from the comparator.

Data Bus I/O Operation (Parallel Mode MC = H)

Pin	Symbol			Function				
22	$\overline{CS}$	H	L	L	L	L	L	L
19	$\overline{WR}$	x	H	L	L	H	H	L
21	$\overline{RD}$	x	H	H	H	L	L	L
20	A0	x	x	H	L	H	L	X
—	Operation		No Operation	Initialize	MPX address setting	High byte read	Low byte read	Inhibit
7	DB7	—	—	DB2 = CODE select	DB2,1,0 = Analog	DB7 ~ DB0	DB7, DB6	
:	:	:	:	H = 2's comp	CH select	= MSB ~ 8th	=9th, LSB	
:	:	:	:	L = binary	0, 0, 0 ~ 1, 1, 1		DB5 ~ DB0	
:	:	:	:	DB1, DB0 = divide ratio	= CH0 ~ CH7		= LOW level	
:	:	:	:	0, 0 ~ 1, 1				
14	DB0	—	—	= 1/1 ~ 1/8				

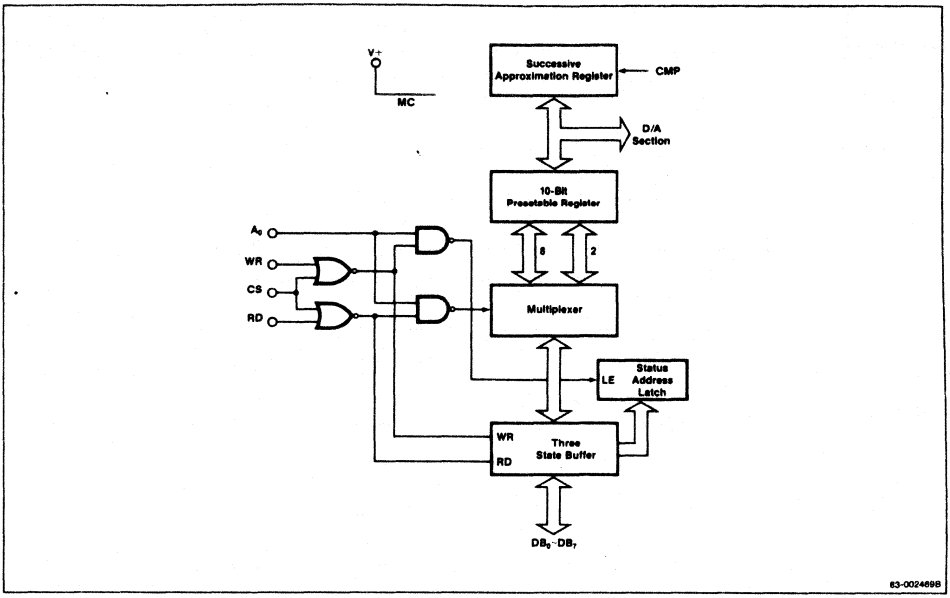
Serial I/O Operation (Serial Mode 1, 2, MC = L)

		Serial Mode 1 (External SCK, A0 = L)		Serial Mode 2 (Signal Processor Mode, A0 = H)	
Pin	Symbol	Direction	Function	Direction	Function
7	SO	O	Serial output (three state). Data are output at the falling edge of $\overline{SCKI}$ or $\overline{SCKO}$.		
8	SI	I	Serial input. Data read at the rising edge of $\overline{SCKI}$ or $\overline{SCKO}$.	I	Tie to V+
9	SC	I	Shift select (H/L — LSB/MSB first)		
10	$\overline{SCKO}$	—	Tie to GND	O	Serial clock output (= internal clock)
11	$\overline{SOEN}$	—	Tie to GND	O	Serial output enable (active low)
12	CODE	I	Code select (H = 2's complement, L = binary)		
13	DIV1	I	Frequency		DIV1, 0 = 0, 0 1,1
14	DIV0	I	Divide ratio setting		= 1/1 1/ 8
19	$\overline{STB}$	I	Address strobe input MPX addresses are latched at the rising edge of $\overline{STB}$ input.	I	Tie to GND
21	$\overline{SCKI}$	I	$\overline{SCKI}$ controls the shift operation of I/O interface shift register. Data are output at the falling edge, and input at the rising edge.	—	Tie to V+
22	$\overline{CS}$	I	Chip select signal input. Low level of $\overline{CS}$ resets the internal sequence, and I/O interface is enabled.	I	Internal sequence reset signal input. Sequence controller are reset at the low level of $\overline{CS}$, and A/D conversion starts at the rising edge of $\overline{CS}$.

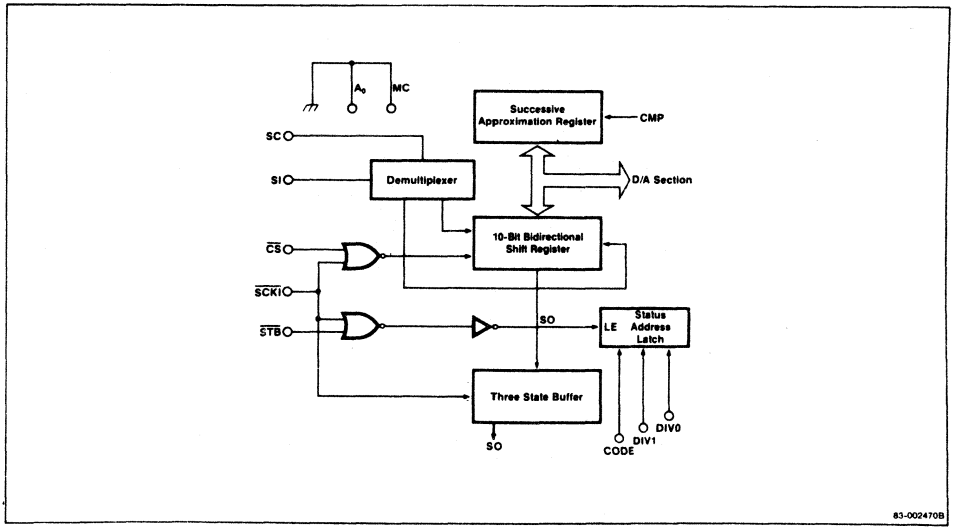
Notes: 1. In serial mode 1. I/O pins listed below are strobed by $\overline{CS}$ signal. Therefore, when $\overline{CS}$ = HIGH, input signals are ignored and output pins are left at high impedance state. Input terminal; SI, $\overline{STB}$, $\overline{SCKI}$ Output terminal; SO

2. In serial mode 2 (signal processor interface mode). By initialization, analog input MPX of CH7 is automatically selected.

Parallel Operation

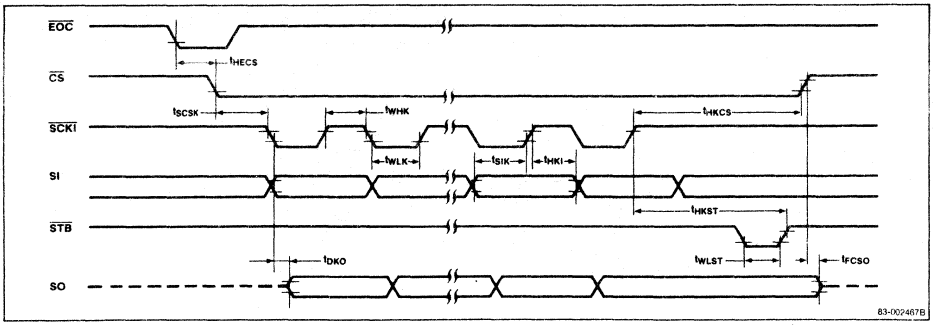


Serial Operation

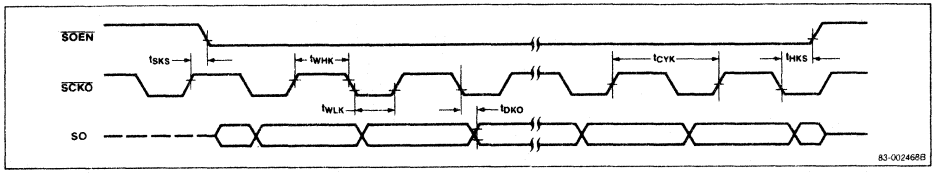


Timing Waveforms

Serial Mode 1

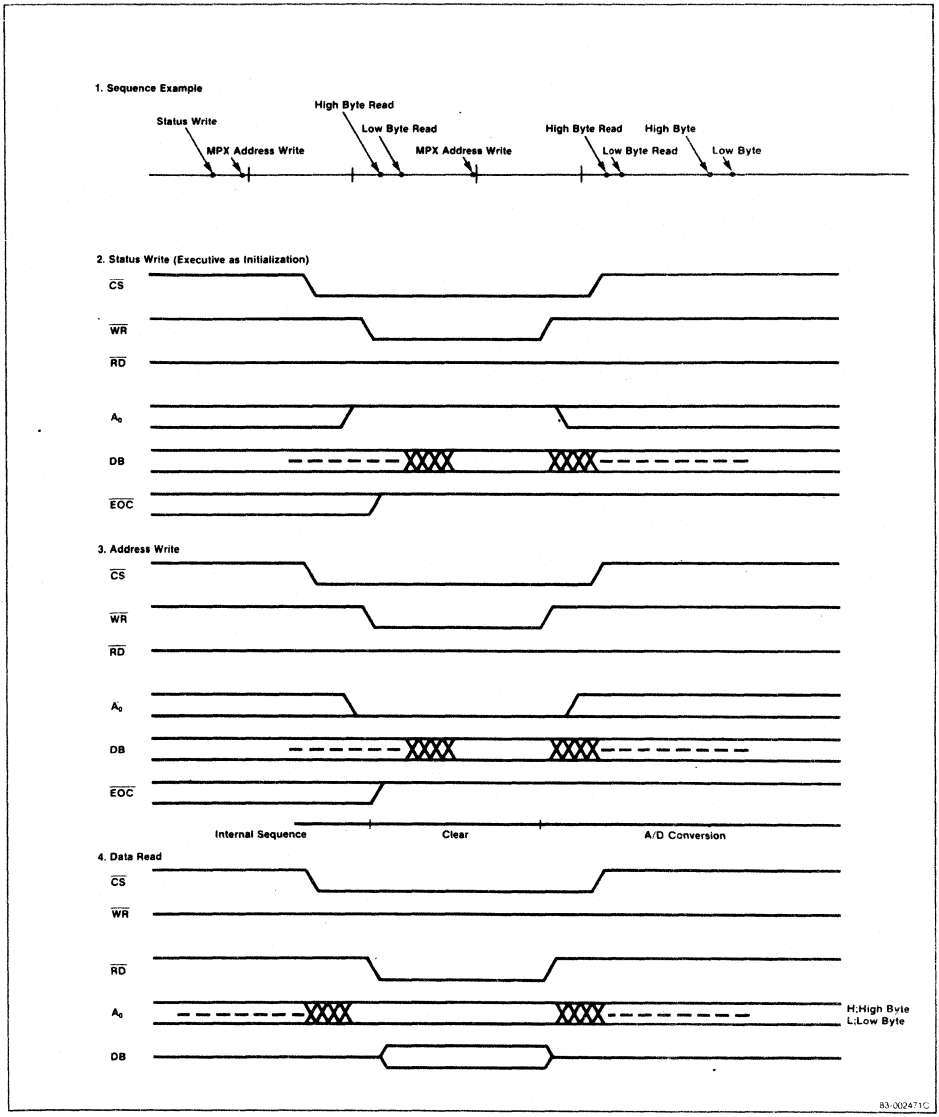


Serial Mode 2



Timing Waveforms (Cont.)

Parallel Mode Timing Chart (MC = H)



APPLICATION NOTES
μPD7003
μPD7004

9/86 V1.0

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Interfacing the A/D-Converter µPD7004 to Microcomputers

μPD7003

1. Outline

The μPD7003 is the high-speed 8-bit A/D converter which contains a resistor network and 256 voltage comparators. The 8-bit digital output is a 3-state parallel output, which allows the μPD7003 to interface easily with microprocessors.

The μPD7003 employs pipe-line processing thereby performing A/D conversion at high speed and outputs the converted data per clock cycle.

However, in the case of the clock ($\overline{CLK}$) signal for A/D conversion and the microprocessor's read signal for data output running independently, read errors may occur when changing points of data conversion fall on the read signals.

This technical document provides the following as an example of the interface which controls the μPD7003 efficiently, without changing the microprocessor's system flow (i.e., without deteriorating the throughput):

(1) Interface using the $\overline{WAIT}$ signal

(2) Interface using the μPD780's/μPD70008's $\overline{M1}$ signal

(3) DMA interface for high-speed data aquisition

For the μPD7003's specification and characteristics, refer to the data sheet.

2. Design and Function of the A/D-Converter μPD7003

The μPD7003's digital interface circuit is structured as that it can be directly connected to the microprocessor's 8-bit bus.
Figure 1 presents the block diagram.

Block Diagram

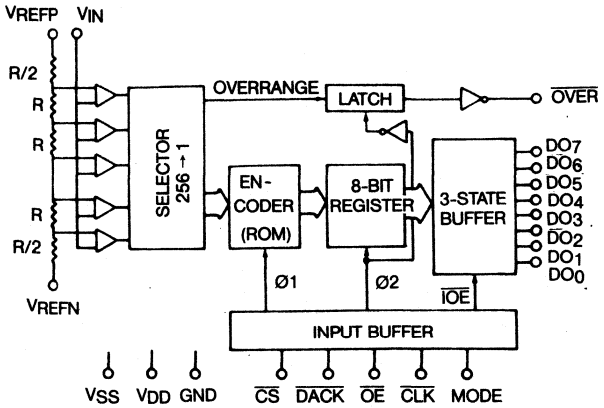


Fig. 1 Block diagram

This digital interface utilies the data bus (DB0 . . . DB7), $\overline{CS}$ and $\overline{OE}$ signals and serves as an interface similar to the microprocessors's peripheral I/O device.

Table 1 shows the function of each pin.

Pin Description

Symbol	Pin Name	Pin. No.	Function
DB0 . . . DB7	Databus	1, 2, 4 . . . 8, 24	The result of the A/D conversion is output to the databus lines with TTL level. The lines stay in a high impedance state at stand-by mode.
$\overline{OVER}$	Overrange	9	Output at the rise time of the CLK signal when the analog input exceeds the range of the voltage range.
$\overline{OE}$	Output enable	18	Output enable signal. Connect with the RD signal of the microcomputer.
$\overline{DACK}$	DMA Acknowledge	17	Input for the DMA signal when using a DMA controller like the μPD8257. If not using the DMA, connect to V_{DD}.
$\overline{CS}$	Chip Select	16	Turn to a low-level for a data read.
$\overline{CLK}$	Clock	15	Controls the timing of the internal circuit. The analog iput is just converted before the rising edge of this signal.
(TEST)	Test .	14	Used for testing the μPD7003. Connect to V_{DD} when desired to use.
MODE	Mode Switch	13	Turns to a serial operation mode on high-level and continiously output at low-level according to the CLK signal.
V_{DD}	Power Supply	10, 12	Power supply pin. Apply +5V.
V_{REF}	Reference Voltage	11	Reference voltage input pin. The input impedance is >12.5 KΩ.
GND	Analog Ground	19,22	Analog ground pin.
V_{SS}	Digital Ground	23	Digital ground pin.
V_{REFN}	Reference Ground	21	Reference ground pin. Sets the lower level of the A/D conversion range. Normally used at the ground level.
V_{IN}	Analog Input	20	Analog input pin.

Table 1: Pin functions

3. A/D CONVERSION AND INTERFACE ERRORS

The μPD7003 employs pipeline processing for high-speed performance and aquires one converted data per clock cycle. Then it is a prerequisite to apply a clock preceding the conversion properly at a certain point in the μPD7003 internal sequence. Therefore, entering a clock more than two cycles in succession is required for the μPD7003 to implement the A/D conversion.

The A/D conversion is always executed upon the $\overline{CLK}$ signal input. When the $\overline{CLK}$ signal and the microprocessor's performance are implemented independently as shown in Figure 2. That is, because there is a possibility for the microprocessor to read incorrect data when the update timing (the fall time of the $\overline{CLK}$ Signal) falls on the rise time of the microprocessor's read signal.

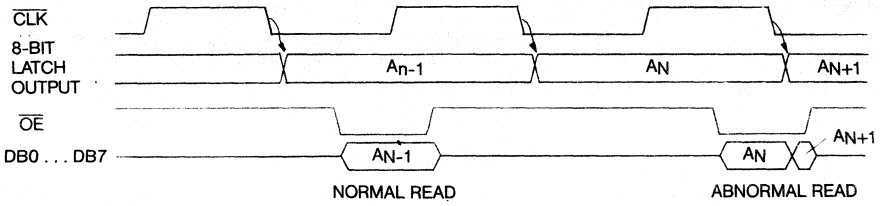


Fig. 2 Read timing

4. INTERFACING THE μPD7003 TO MICROPROCESSOR-SYSTEM

Shown below are the examples of the interface, which effectively eliminates such read errors of the microprocessor as mentioned above.

4.1 An Interface Using the $\overline{\text{WAIT}}$ Signal

Figure 3 presents an example of an effective interface circuit, using the $\overline{\text{WAIT}}$ signal of the μPD780 or μPD70008.

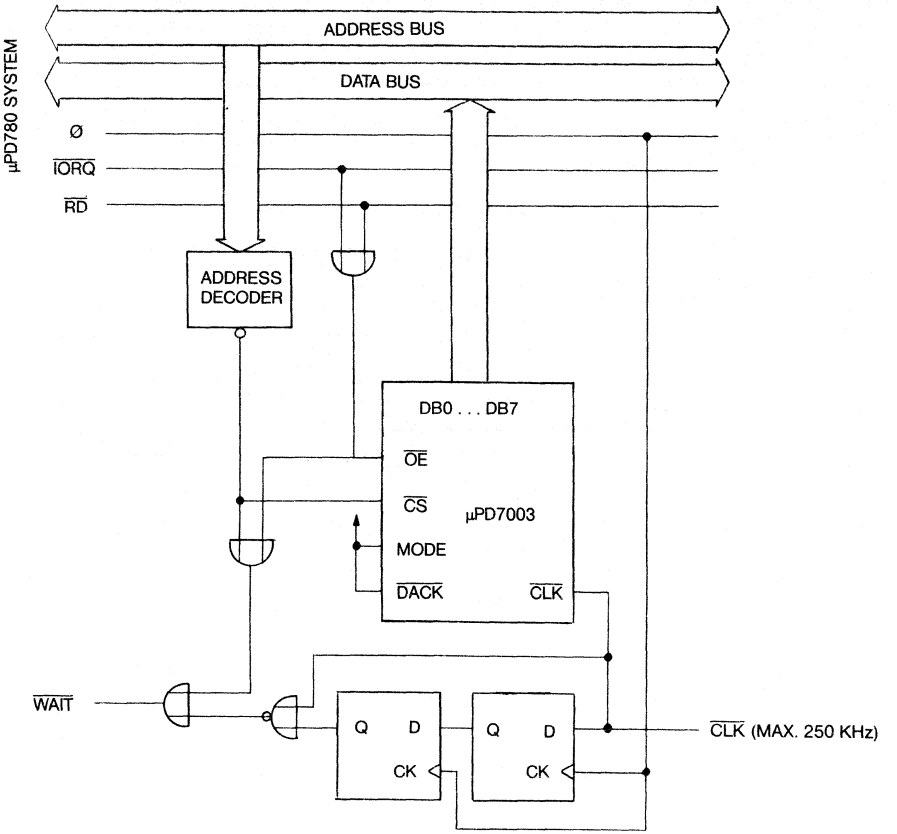


Fig. 3 Interface circuit using WAIT signal

In the circuit shown above, the PD780's I/O read cycle is being executed while the clock signal ($\overline{CLK}$), entered to the μPD7003, is in a high level. It applies the $\overline{WAIT}$ signal to the μPD780, thereby turning the $\overline{CLK}$ signal to fall, and allowing the μPD780 to read data. Figure 4 indicates the timing.

The $\overline{CLK}$ signal shown in Figure 3 is delayed two cycles by sampling it with the system clock.

Using this circuit generates a variation up to 2 μs in the I/O read cycle execution time depending on the level (high or low) at which the cycle is implemented. Nevertheless, the circuit is very favorable, having no restrictions to the μPD780's software, and thus causes no troubles in programming.

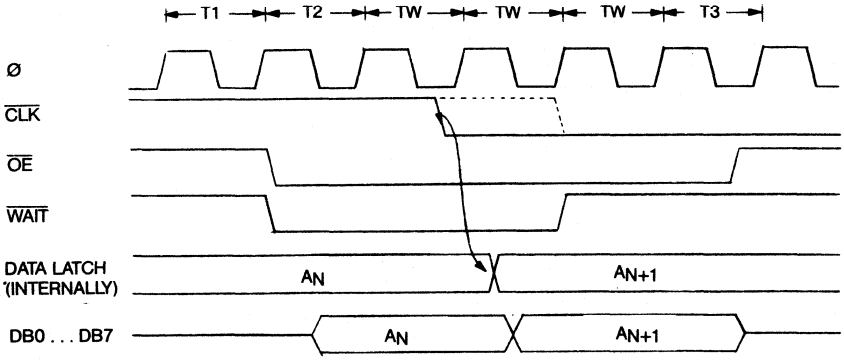


Fig. 4 Read timing (WAIT)

4.2 An Interface Using the $\overline{M1}$ Signal

The interface described below is as effective as the one shown in chapter 4.1. It enters the CLK signal to the μPD7003, from the M1-signal which is output from the μPD780/70008. An example of this circuit is given in Figure 5.

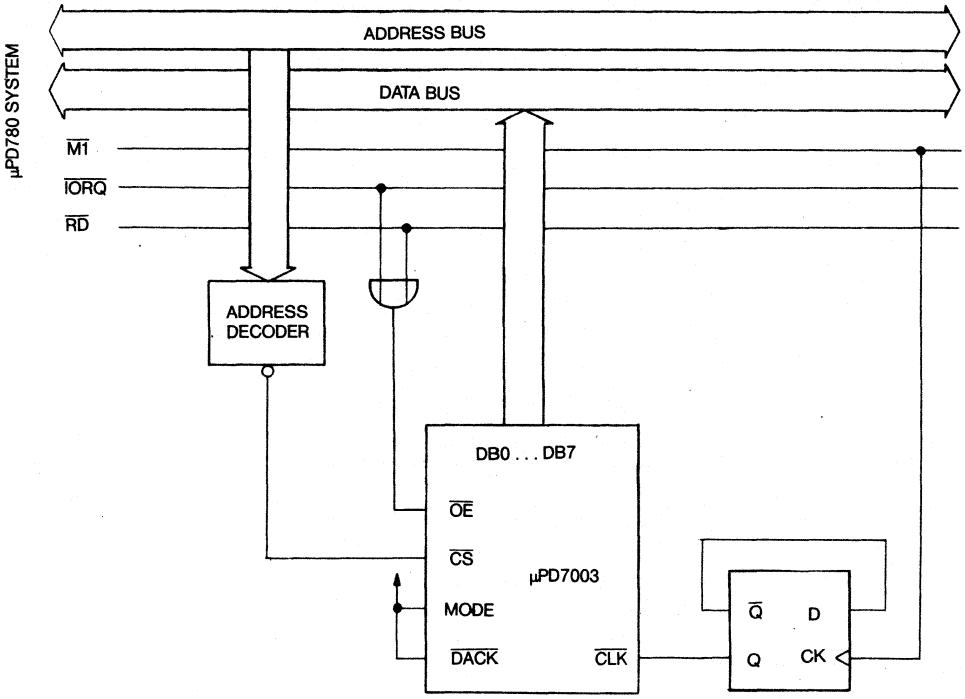


Fig. 5 Interface circuit using $\overline{M1}$ signal

In this example, the $\overline{M1}$ signal which is output at the first cycle (OP-Code Fetch Cycle) of each instruction of the μPD780 is used, after dividing into two, as the $\overline{CLK}$ signal for the μPD7003. The timing for the A/D converted data read (during the I/O Read cycle) avoids falling on the changing point of the $\overline{CLK}$ signal (during the OP fetch cycle), since they operate in different cycle periods as shown in Figure 6.

In addition, the division of the $\overline{M1}$ signal being implemented at the rise time of itself, provides a surplus in the rise time of the $\overline{OE}$ signal to the changing point of the $\overline{CLK}$ signal. The timing is shown in Figure 6.

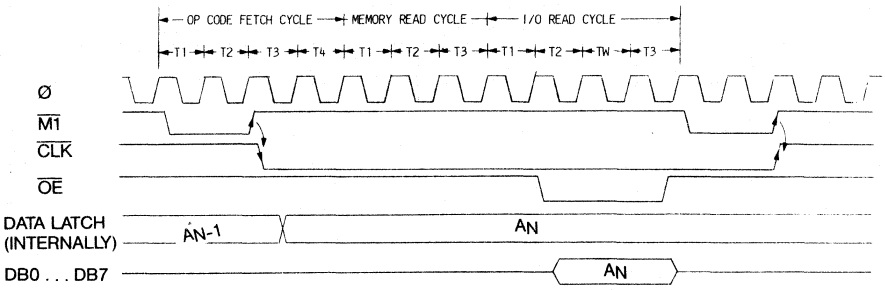


Fig. 6 Timing for IN instruction execution

This circuit, however, cannot satisfy the requirement for the μPD7003's clock if the microprocessor's instruction cycle is less than 2 μs. This is because one instruction cycle of the μPD780 is equivalent to half the conversion cycle of the μPD7003.

Note, also, that the μPD7003 achieves conversion in pipe-line processing, and more than two cycles of the $\overline{CLK}$ signal are required to aquire one A/D converted data. Therefore, each of the three instructions preceding the IN instruction (by which the μPD780 reads the converted data) need to use more than 2 μs for its execution.

To avoid such complicated handling of the instruction selection, one more frequency divider 74LS74 (shown in Figure 5) may be added, thereby making the division ratio 1/4.

4.3 An Example of DMA Interfacing

An Example of the interface which handles high-speed data aquisition using DMA transfer, is presented in Figure 7.

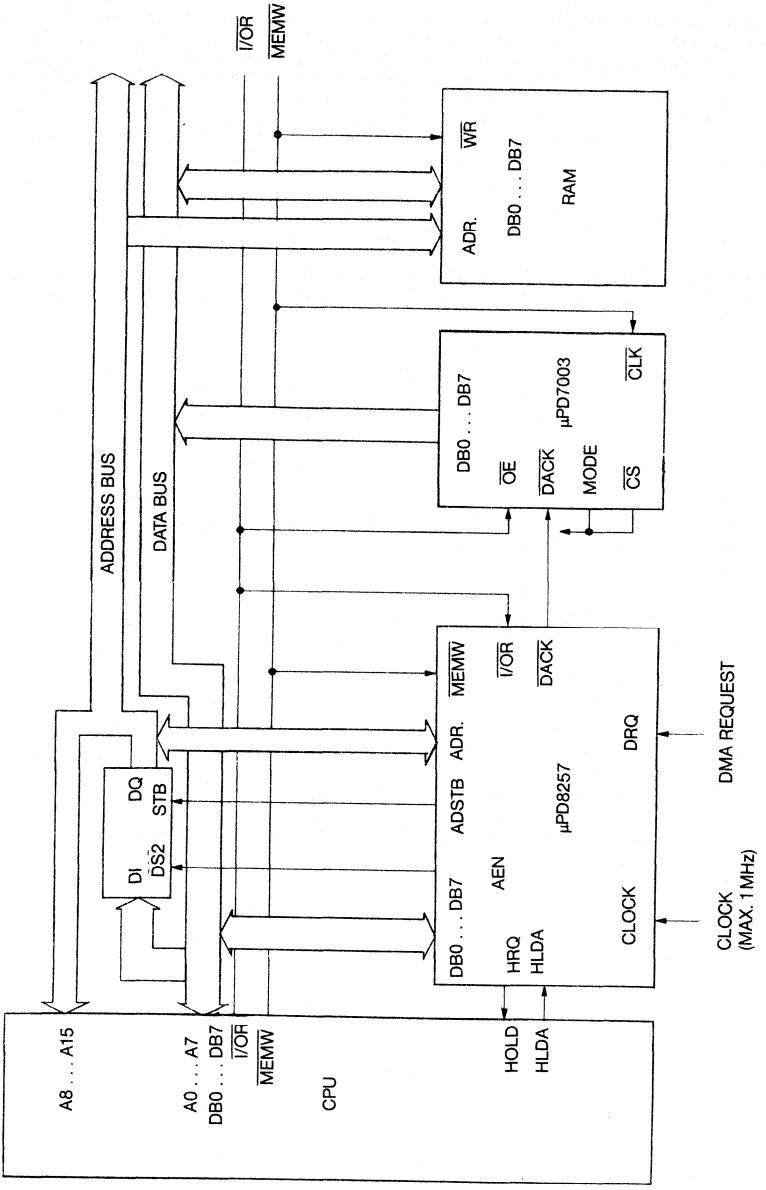


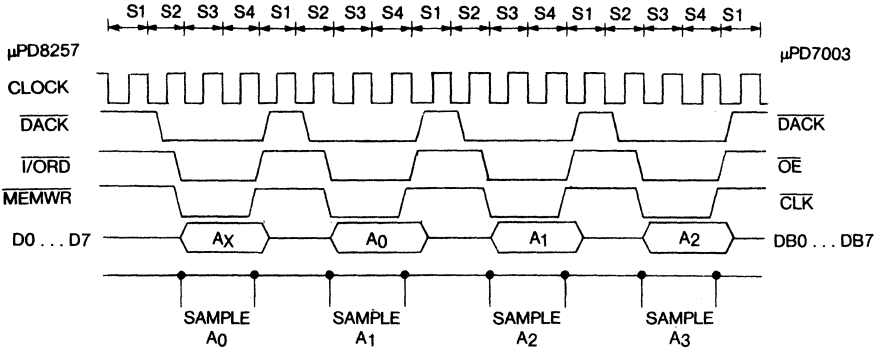
Fig. 7 DMA interface block diagram

In the example above, the data converted by the μPD7003 is directly transfered to memory by use of the DMA controller μPD8257. The memory write signal ($\overline{MEMW}$) which is output at the a clock to designate the μPD8257, is used in a extended write mode as a clock to designate the μPD7003's conversion cycle. By employing the extended write mode, the $\overline{MEMW}$ signal becomes halfdutied and is output from the μPD8257 at the DMA block transfer time. In addition, the $\overline{MEMW}$ signal runs synchronously with the $\overline{OE}$ signal (μPD8257's I/OR signal output) thereby eliminating such read errors mentioned before.

The DMA start is commenced by externally entering the DMA request signal to the μPD8257. Then the CPU turns to a hold state and the DMA transfer first brings invalid data. Valid data is offered from the second transfer like shown in figure 8 timing chart.

In the example mentioned below, the μPD8257's $\overline{MEMW}$ signal, of which maximum frequency is 250 kHz, is used as a clock for the μPD7003. This means that the maximum CLOCK signal input from the μPD8257 is 1 MHz.

The system with the DMA controller is convenient for analyzing analog information since it performs sampling in a periodic cycle, while each system explained in 4.1 and 4.2 achieves sampling upon each instruction execution by the microprocessor.



*: Extended write mode
AX: Invalid Data

Fig. 8 DMA transfer timing

μPD7004

1. OUTLINE

μPD7004 is a single chip, 10-bit A/D converter which contains an 8-channel analog-input multiplexer and a microcomputer interface circuit.

The support twp kinds of serials modes and a 8-bit parallel mode, which enables the μPD7004 to be easily connected to many kinds of microcomputers like Single-Chip-Microcomputers (μCOM75, μCOM84, μCOM87), Multi Chip-Microcomputers (μPD780, μPD8085, μPD70008, etc.) or Signal Processors (μPD7720).

The following interface examples are given in the rest of this note:

(1) Interfacing with an 8-bit Microprocessor

(2) Serial interface with a single-chip microcomputer

(3) Interfacing with signal processor μPD7720

For the μPD7004 specifications and characteristics, please refer to the data sheet.

2. DESIGN AND FUNCTION OF THE A/D CONVERTER μPD7004

Figure 1 shows the μPD7004 block diagram. The function of each terminal is described in Table 1.

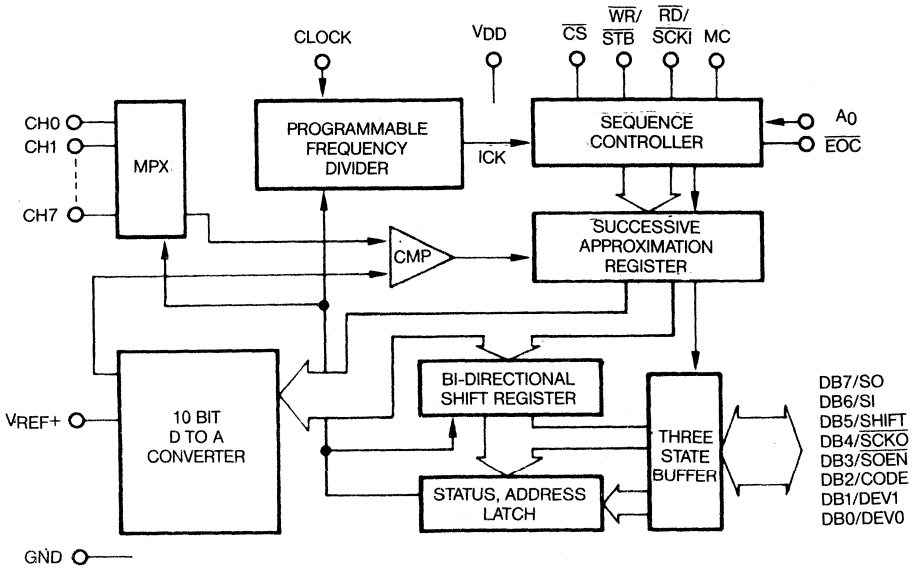


Fig. 1 μPD7004 Block Diagram

PIN NO.	SYMBOL	PARALLEL MODE	SERIAL MODE
		FUNCTION	FUNCTION
1	CH4	Analog Input CH4	
2	CH5	Analog Input CH5	
3	CH6	Analog Input CH6	
4	CH7	Analog Input CH7	
5	Vref+	Positive Reference Voltage Input	
6	GND	Ground Digital	
7	DB7/SO	Data Bus (MSB)	Serial Output
8	DB6/SI	Data Bus (2nd)	Serial Input
9	DB5/SHIFT	Data Bus (3rd)	First Bit Select (LSB/MSB)
10	DB4/$\overline{SCK0}$	Data Bus (4th)	Serial Clock Output
11	DB3/$\overline{SEON}$	Data Bus (5th)	Serial Output Enable
12	DB2/CODE	Data Bus (6th)	Code Select
13	DB1/DEV1	Data Bus (7th)	Freq. Divide Ratio Set
14	DB0/DEV0	Data Bus (LSB)	Freq. Divide Ratio Set
15	VDD	Power Supply Digital	
16	$\overline{EOC}$	End of Conversion (Active Low)	
17	CLOCK	Clock Input (f_{CLK})	
18	MC	MODE Select (H = Parallel, L = Serial)	
19	$\overline{WR}/\overline{STB}$	Write	Address Write Strobe
20	AO	Control Address	Internal/External Shift Clock
21	$\overline{RD}/\overline{SCKI}$	Read	Serial Clock Input
22	$\overline{CS}$	Chip Select	
23	VDD	Power Supply Analog	
24	GND	Ground Analog	
25	CH0	Analog Input CH0	
26	CH1	Analog Input CH1	
27	CH2	Analog Input CH2	
28	CH3	Analog Input CH3	

Table 1 Terminal Functions

The microcomputer interface circuit is able to operate in different modes, depending on the value on the mode selection terminal and the A0 pin as shown in table 1. The serial mode supports two modes:
Serial mode 1 is used for the microprocessor serial interface, and serial mode 2 for the signal processor (μPD7720).
The selection of mode 1 or 2 is performed through the address input pin A0. Table 2 described the performance of the multi-function terminal.

SYMBOL	PIN NO.	SERIAL MODE 1 (EXTERNAL SERIAL CLOCK, A_0 = L) I/O	SERIAL MODE 1 PERFORMANCE	SERIAL MODE 2 (SIGNAL PROCESSOR MODE, A_0= H) I/O	SERIAL MODE 2 PERFORMANCE
SO	7	Output	Serial Output (3-state) To be output synchronously during the fall time of the $\overline{SCKI}$ or $\overline{SCKO}$ signal.		
SI	8	Input	Serial Input To be read synchronously during the rise time of the $\overline{SCKI}$ signal.	Input	To be connected to V_{DD}
SHIFT	9	Input	Shift Select (H: LSB first; L: MSB first)		
$\overline{SCKO}$	10	–	To be connected to ground potential	Output	Serial Clock Output (= Internal Clock)
$\overline{SOEN}$	11	–	To be connected to ground potential	Output	Serial-Out Enable (= Active Low)
CODE	12	Input	Code Select (H = 2's complement, L = Binary)		
DEV_1	13	Input	Division Ratio Set		
DEV_0	14	Input			
$\overline{STB}$	19	Input	Address Strobe Signal Reads address data to the address latch during the rise time.	Input	To be connected to ground potential
$\overline{SCKI}$	21	Input	Control signal for the Interface Shift Register. To be output during the fall time and input during the rise time.	–	To be connected to V_{DD}
$\overline{CS}$	22	Input	Chip Select Signal Resets the internal sequence. Serves as an interface at the low-level, thereby allowing data input/output.	Input	Internal Sequence Reset Signal Resets the sequence controller at the low-level, starts the A/D conversion at the rise time.

DEV_1	L	L	H	H	
DEV_0	L	H	L	H	
Division Ratio	1/1	1/2	1/4	1/8	

Notes: 1. In Serial mode 1, the following signals are strobed by the $\overline{CS}$ signal. Therefore, the output signals are ignored and the output pins becomes high impedance when $\overline{CS}$ = HIGH.

Input pin: SI, $\overline{STB}$, $\overline{SCKI}$
Output pin: SO:

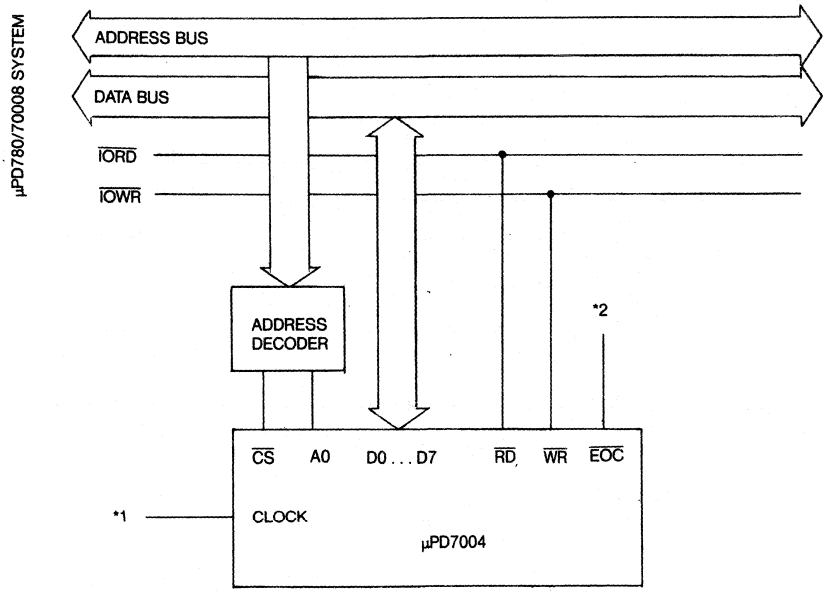
2. In serial mode 2, the internal sequence reset signal $\overline{CS}$ specifies CH_7.

Table 2 Multi-Function Terminal Performance

3. AN EXAMPLE OF PARALLEL MODE INTERFACING TO THE μPD780

Figure 2 shows an example of connecting the μPD7004 to a μPD780/μPD70008 microprocessor system. As shown in this diagramm, in the parallel mode the device is connected like a LSI microcomputer peripheral.

In this example, the μPD780 is employed as a CPU. It is also possible to have other 8-bit CPUs such as the μPD8085A connected in the same logic design, with some timing management by the wait cycle.



*1 Can be used for interruption request signals to the CPU.
*2 Can apply a clock to the CPU.

Fig. 2 Diagram of a system using μPD780 and μPD7004 in parallel mode

The performance of μPD7004 in this mode is controlled by the CPU. The basic sequence is shown in Figure 3 and the CPU flow chart in Figure 4.

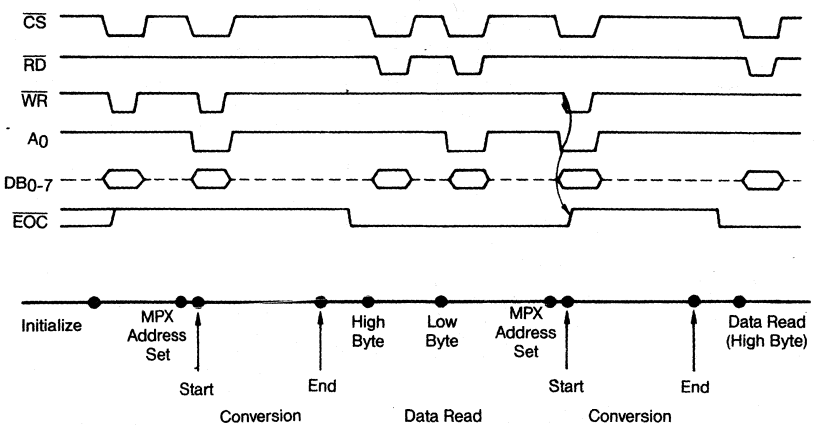


Fig. 3 Example of parallel mode sequence

At initialization, the division ratio of the externally entered clock signal and the conversion code are specified. There is a choice of four division ratios: 1/1, 1/2, 1/4 and 1/8. It is also possible to apply the μPD780 system clock.

The A/D conversion starts by writing the analog multiplexer address. This requires 96 – 104 μs when the clock is 1. MHz. The μPD7004 sends an End-of-Conversion-Signal ($\overline{EOC}$) when the device has executed the conversion. This signal is normally used as an interrupt request signal to start the read procedure.

The converted data is read through the 8-bit bus; the high-order 8 bits of the data are read as a high byte and the last two bits as a low byte. This converted data is latched internally in the μPD7004 and can be read whenever required.

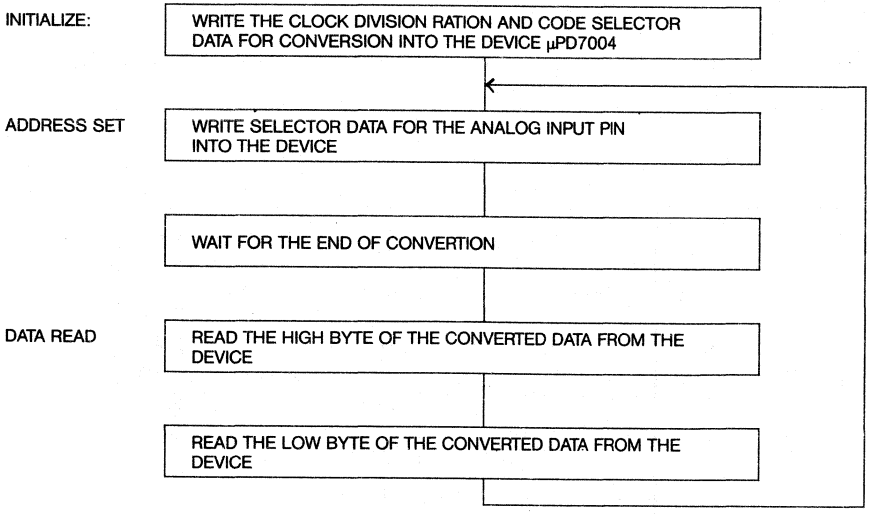


Fig. 4 Parallel Mode Flow Chart

4. INTERFACING IN SERIAL MODE 1

Compared to the parallel mode, the serial mode has the advantage when used in connection with single-chip microcomputers since fewer signal lines are required.

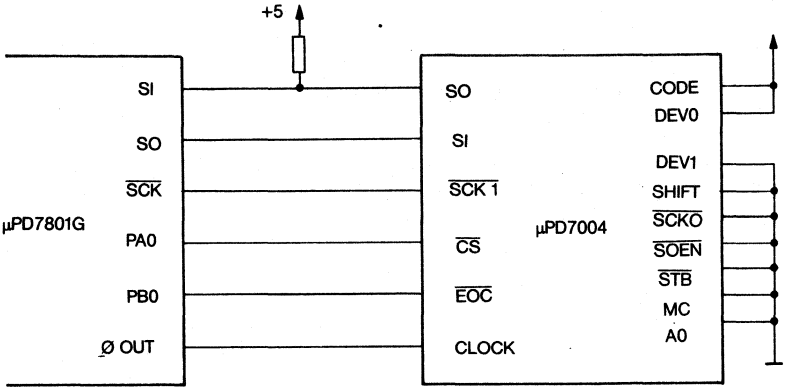
In the serial mode, it is not necessary to set the division ratio or to select the conversation data because this is done by the fixed connection between the specific termininals. Performance in serial mode is described below.
The performance of the μPD7004 is controlled by the $\overline{CS}$ signal. When the CS signal is in the active state ($\overline{CS}$ = "0"), serial data transfer can be achieved. The A/D conversion starts when the $\overline{CS}$ signal starts to rise. The A/D conversion takes 96 – 104 μs when the clock is 1 MHz, the same as in the parallel mode.

When the A/D conversion has been completed, the $\overline{EOC}$ signal changes to the low level to notify the end of the conversion. Then the CPU, after confirming this signal, performs serial data transfer to read the converted data and to set the analog multiplexer's address.

The following examples show the connection of the μPD7004 in the serial mode 1 and the 8-bit single-chip microcomputer μPD7801 and also a connection to the 4-bit single-chip microcomputer μPD7519.

4.1 An Example of Interfacing with the 8 Bit Microcomputer μPD7801

Figure 5 shows an example of the interface with the μPD7801.

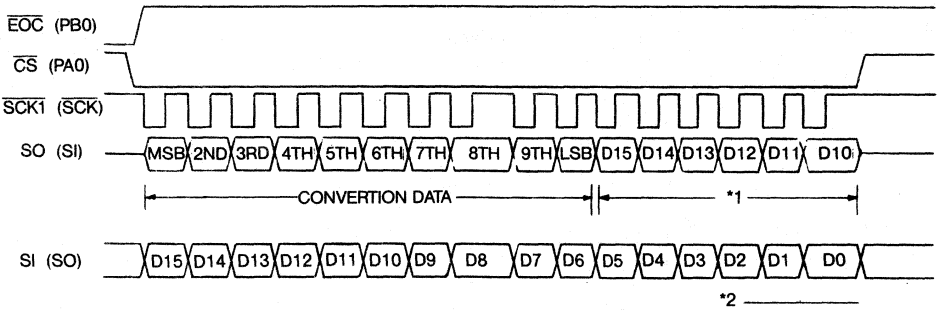


Transfer Serial Mode 1
MSB First
2's Complement Code
Division Ratio 1/2

Fig. 5 μPD7004/μPD7801 connection

The μPD7801 contains a serial interface circuit and handles 8-bit data transfer. Therefore, the μPD7801 performs 8-bit data transfer twice to handle the μPD7004C's 10-bit serial data transfer. The timing of the data transfer is showing in Figure 6.

The μPD7004's 10-bit shift resister is a two-way shift resister, and outputs the data entered through the SI terminal directly from the SO terminal when a serial clock of over 11 bits is entered. That is, the SO terminal of the μPD7004 continuously outputs 10-bit converted data and data entered through the SI terminal (D15 . . . D0 in Figure 6) when the 8-bit transfers are performed twice.



*1 The data entered through the SI terminal is output.
*2 Channel selector data is latched during the rise time of the $\overline{CS}$ signal when the $\overline{STB}$ signal is fixed at the low level.

Channel selector data

D2	L	L	L	L	H	H	H	H
D1	L	L	H	H	L	L	H	H
D0	L	H	L	H	L	H	L	H
Channel	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7

Fig. 6 Timing in serial mode 1 (connection with μPD7801)

In this example, reading the conversion data and selecting the analog multiplexer channel are performed at the same time. Note, however, that the data aquired through the first serial transfer after the power supply is turned on is invalid.

An example of the program is given below.

Example 1:

```
Channel Selector Data Set
CHAN:   ORI   PA, 1       ; Make CS of the μPD7004C HIGH.
        LXI   H, ADCH     ; Set the storage address for channel selector data.
        LDAX  H+
        MOV   S, A        ; Channel Selector Data
        ANI   PA, OFEH    ; Make CS of the μPD7004C LOW.
        SIO               ; Transfer Start
        JR    S-2
        ORI   PA, 01      ; Make CS of the μPD7004C HIGH.

Converted Data read/Channel Data Set
ADCNV:  LXI   D, ADCR     ; Data Pointer Set
CKEOC:  OFFI  PB, 01H     ; EOC = 0?
        JR    CKEOC
        MVI   A, 0
        MOV   S, A        ; Set first serial output data to 0
        ANI   PA, OFEH    ; Make CS of the μPD7004C LOW.
        SIO               ; First Transfer Start
        SKIT  FS
        JR    S-2
        MOV   A, S        ; Fetch the 8 high-order bits (MSB-8th) of the converted data.
        STAX  D+          ; Store the converted data.
        LDAX  H+          ; Load the next channel selector data.
        MOV   S, A
        SIO               ; Second Transfer Start
        SKIT  FS
        JR    S-2
        ORI   PA, 01H     ; Make CS of the μPD7004C HIGH.
        MOV   A, S        ; Fetch the 2 low-order bits (9th, LSB, 0 . . .0) of the converted data.
        STAX  D+          ; Store the converted data.
```

4.2 An Example of Interfacing with the 4-Bit-Microcomputer μPD7519/7519H

Figure 7 shows an example of the interface with the μPD7519. The serial operation of the μPD7519 is performed in the system block mode in this example. The shift terminal of the μPD7004 changes to LOW since the μPD7500 series performs the MSB-first shift operation.

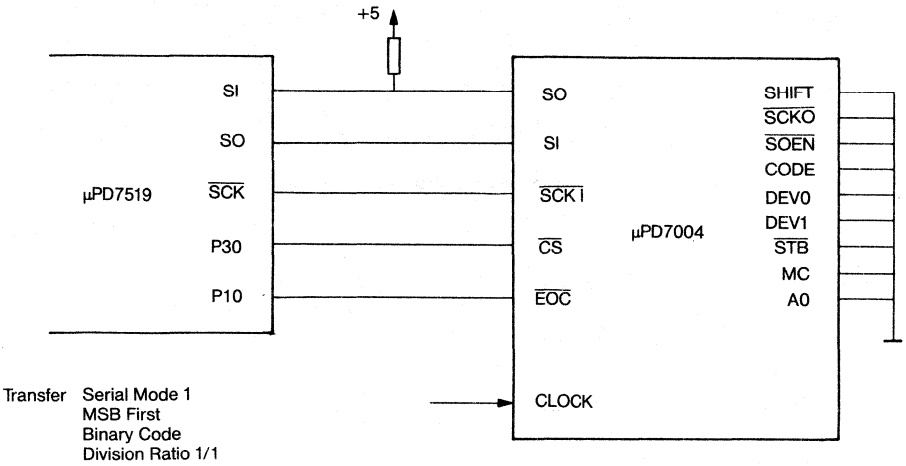


Fig. 7 μPD7004/μPD7519 Connection

The serial transfer function of the μPD7500 series performs 8-bit transfers like the μPD7801 as shown in 4.1 and is also required to perform serial transfers twice to fetch data. The analog channel selection and the conversion data read are described with an example in the following subsection.

(1) Analog channel selection
The analog channel selection is achieved with an 8-bit serial transfer as shown in Figure 8; the last three bits (LSB – 6th) of the serial input data serve as channel selector data. That is, the channel selector data for conversion is set in the μPD7519's shift register before the SIO instruction is executed.

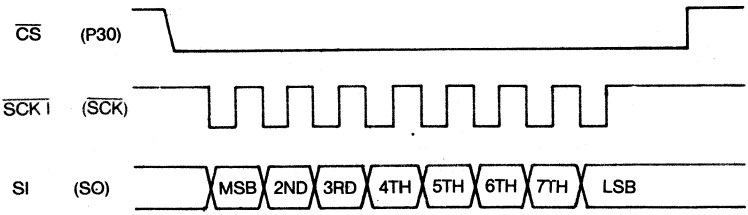


Fig. 8 Timing of channel selector data transfer

The program for the channel selection is shown in Example 2.

Example 2: Program for channel selection

```
CHAN:   LHLI ADCH       ; ADCH stores channel data for the next reference
        TAMSIO
        SIO
        IDRS ADCH       ; Channel no. increment
        NOP
```

(2) Conversion data input

Fetching the converted data requires a special operation because it is 10-bit data. The timing chart for this is given in Figure 9. An example of the program is shown in Example 3.

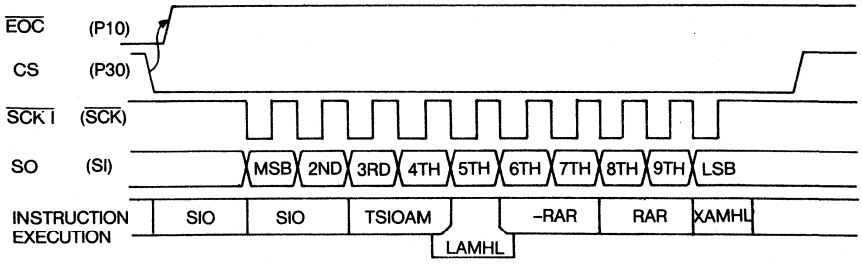
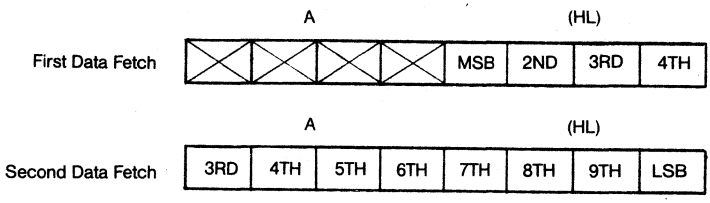


Fig. 9 Timing chart for conversion data input

```
Example 3: Program for conversion data input
ADCONV:  LHL1   CDATA      ; Data Pointer Set
EOC:     IP1               ; EOC Check
         CMA
         SKABT 0
         JCP    EOC
         ANP    3,1110B    ; CS+L
         SIO               ; Serial Transfer Start
         SIO               ; Serial Transfer Restart
         TSIOAM            ; Serail Data Fetch (1st)
         LAM    HL         ; Data Adjustment
         RC
         RAR
         RC
         RAR
         XAM    HL         ; Data Store
         DLS
         TSIOAM            ; Serial Data Fetch (2nd)
         ILS
         ST     ; Data Store
```



In the example above, fetching the 10-bit data is done by performing the SIO instruction twice in succession. The first SIO instruction issues two serial clock pulses and the second SIO instruction eight pulses. Thus, the contents of the μPD7519's shift register, consisting of 8-bit, are to be read internally in the midtH of the μPD7004's 10-bit serial transfer.

In the program shown above, the first TSIOAM instruction following the second SIO instruction reads the four high-order bits (MSB – 4th) of the converted data and the second TSIOAM instruction reads eight bits (3rd – LSB). The second reading of the two bits (the 3rd and 4th) in the execution of the two TSIOAM instructions is adjusted by the shift right instruction.

5. INTERFACE IN SERIAL MODE 2

In serial mode 2 direct connection can be made to the digital signal processor (μPD7720) and A/D converter. Unlike the above mentioned parallel mode and serial mode 1, it is performed in a periodic cycle.

Signals in the interface, unlike with serial mode 1, are controlled by the μPD7004. Figure 10 shows an example of connecting the μPD7004 to the μPD7720.

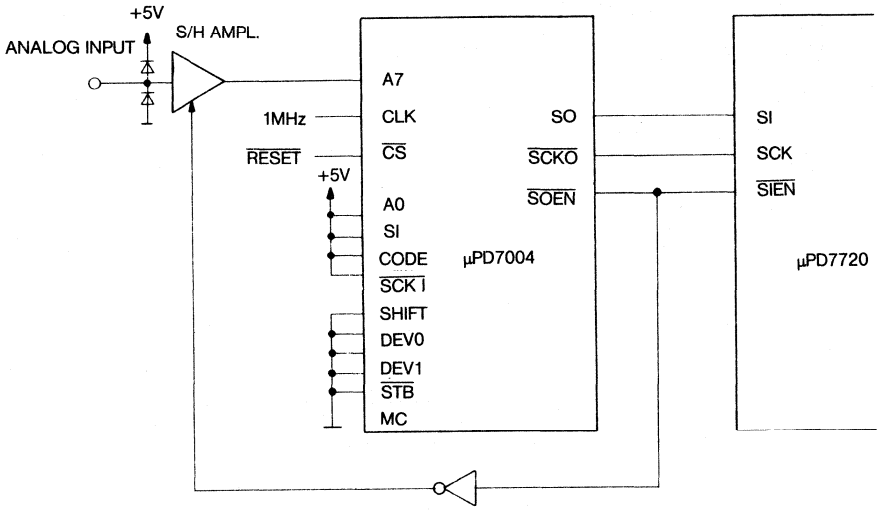


Fig. 10 μPD7004/μPD7720 connection

As shown in Figure 10, it is possible to interface with only three signal lines in serial mode 2. A/D conversion is performed every 104 μs (when clock = 1MHz). The converted data is output synchronously with the $\overline{SOEN}$ signal.

The μPD7720's serial interface performs 16-bit data transfer, while the converted data consists of 10 bits. Therefore, 6 bits of high dat automatically follow the 10 bits of converted data.
Figure 11 shows the timing chart for this example.

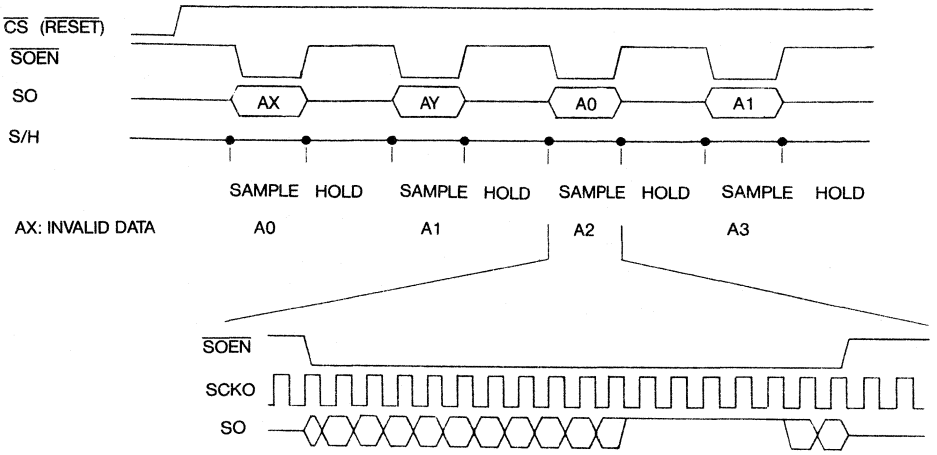


Fig. 11 Timing chart

In the example above, an external sample/hold circuit is used and the whole operation is performed as a kind of pipe-line processing. The $\overline{SOEN}$ signal supplies valid data three cycles after the reset cancellation, and then supplies converted data every 104 μs after this.

Description

The μPC398 is a monolithic sample and hold circuit which combines J-FET and bipolar circuitry on the same substrate to provide a high input impedance input buffer and a high speed output buffer. Operating as a unity gain input buffer circuit, DC accuracy is typically 0.004% and acquisition time is as low as 6 μs with a maximum gain error of 0.01 %. This device is ideal for data acquisition circuits requiring high speed and high input impedance.

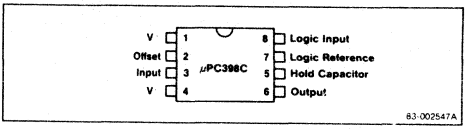
Features

- ☐ Fast acquisition time
- ☐ Gain accuracy: 0.004%
- ☐ Input offset voltage: 2 mV
- ☐ Direct interface to TTL/CMOS
- ☐ LF398 direct replacement

Ordering Information

Part Number	Package	Temperature Range
μPC398C	Plastic DIP	−20 °C to +70 °C

Pin Configuration



Absolute Maximum Ratings

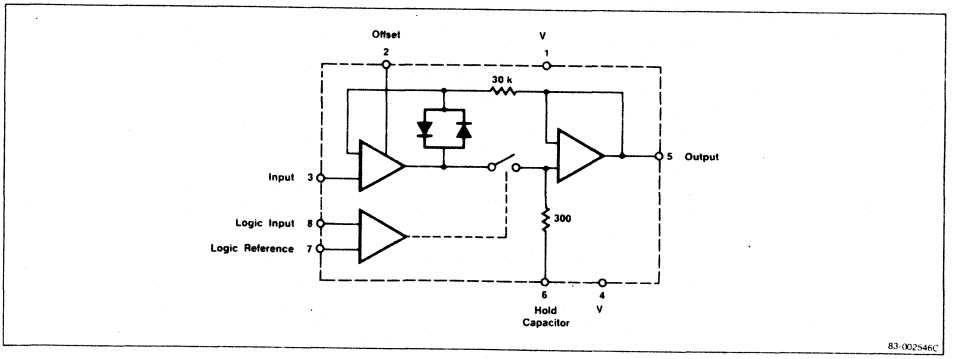
$T_A = 25\,°C$

Voltage Between V+ and V−	36 V
Input Voltage Range (Note 1)	±15 V
Logic to Logic Reference Differential Voltage	−0.3 to +7.0 V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 s
Power Dissipation	350 mW
Operating Temperature Range	−20 to +70 °C
Storage Temperature Range	−55 to +150 °C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Equivalent Circuit

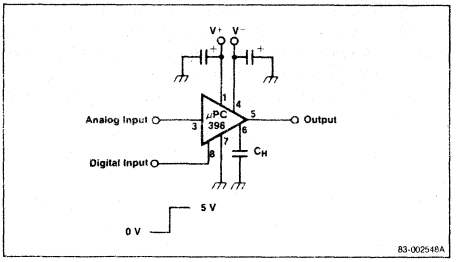


Recommended Operating Conditions

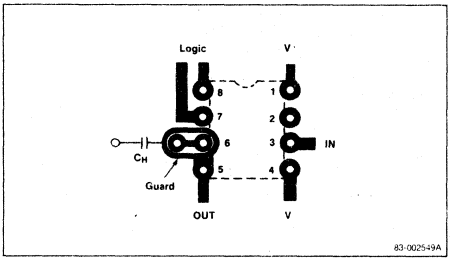
$T_A = 25°C$, $V^{\pm} = \pm 15$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Voltage	$V^{\pm}$	±5	±15	±16.5	V	
Analog Input Voltage	V_{IN}	−11.5		+11.5	V	
Sample Mode Logic Input Voltage	V_{SH}	2.7		5.25	V	$V_{REF} = 0$
Hold Mode Logic Input Voltage	V_{SH}	−15		0.5	V	$V_{REF} = 0$
Logic Input Voltage Slew Rate	SR	0.2			V/μs	
Hold Capacitor	C_H	0.001		0.1	μF	

Typical Connection



Guarding Technique (Bottom View)



Electrical Characteristics

$T_A = 25°C$, $V^{\pm} = \pm 15$ V, $-11.5\ V \le V_{IN} \le +11.5$ V, $C_H = 0.01\ \mu F$, $R_L = 10\ k\Omega$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input Offset Voltage	V_{io}			7.0	mV	
Input Bias Current	I_b			50	nA	
Input Impedance	R_{IN}		10^{10}		Ω	
Gain Error				0.01	%	
Feedthrough Attenuation Ratio		80			dB	f = 1 kHz
Output Impedance	Z_0			4.0	Ω	
Hold Step Voltage	V_{HS}			2.5	mV	$V_O = 0$
Leakage Current into Hold Capacitor	I_{OLK}			200	pA	$V^{\pm} = \pm 5$ V to ±18 V
Acquisition Time	t_{aq}		4		μs	$\Delta V_O = 10$ V, 0.1% Error, $C_H = 1000$ pF
	t_{sq}		20		μs	$\Delta V_O = 10$ V, 0.1% Error, $C_H = 0.01$ pF
Hold Capacitor Charging Current	I_{CH}		5		mA	$V_{IN} \leftarrow V_O = 2$ V
Logic Input Current	I_{IN}			10	μA	
Logic Threshold	V_{TH}	0.8		2.4	V	
Supply Voltage Rejection Ratio	SVRR	80			dB	
Supply Current	I_{CC}			±6.5	mA	$V^{\pm} = \pm 15$ V to ±18 V

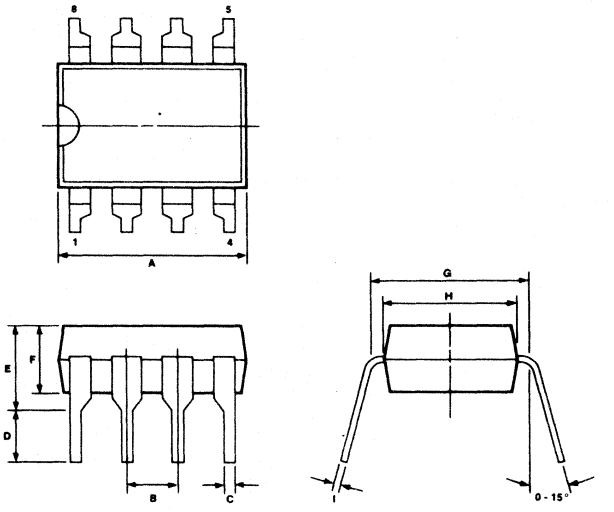
PACKAGING INFORMATION

Packaging Information

8-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	10.5 max	.413 max
B	2.54 [TP]	.100 [TP]
C	.5	.002
D	2.7 min	.106
E	5.90 max	.228
F	.5	.002
G	6.40 [TP]	.252 [TP]
H	7.62	.300
I	.25	.010

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "G" to center of leads when formed parallel.

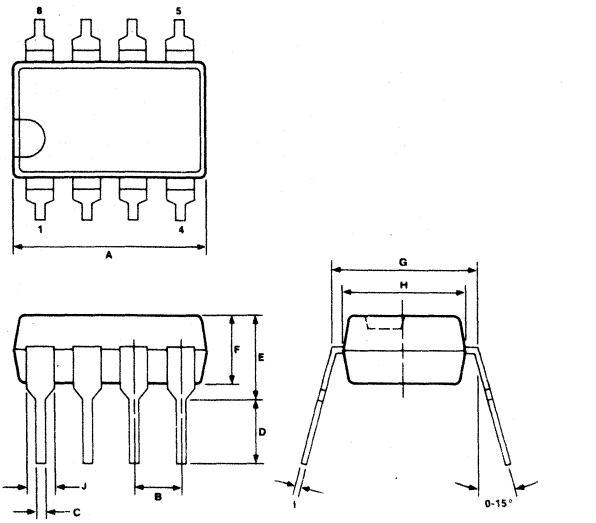


83-003392B

8-Pin Plastic DIP (300 mil) (μPC3423 only)

Item	Millimeters	Inches
A	10.5 max	.413
B	2.54 [TP]	.100 [TP]
C	.5	.002
D	3.5	.138
E	4.7	.185
F	3.8	.150
G	6.40 [TP]	.252 [TP]
H	7.6	.299
I	ø .3	.012
J	1.2	.047

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "G" to center of leads when formed parallel.

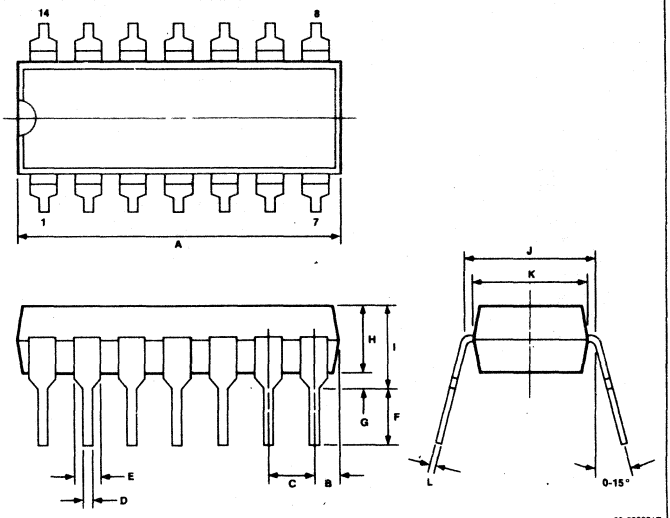


83-003395B

14-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	1.2 min	.047 min
F	3.6 ± 0.3	.142 ± .012
G	.51 min	.020 min
H	4.31 max	.170 max
I	5.08 max	.200 max
J	7.62 [TP]	.300 [TP]
K	6.4	.252
L	.25 $^{+.10}_{+.05}$	.010 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "J" to center of leads when formed parallel.

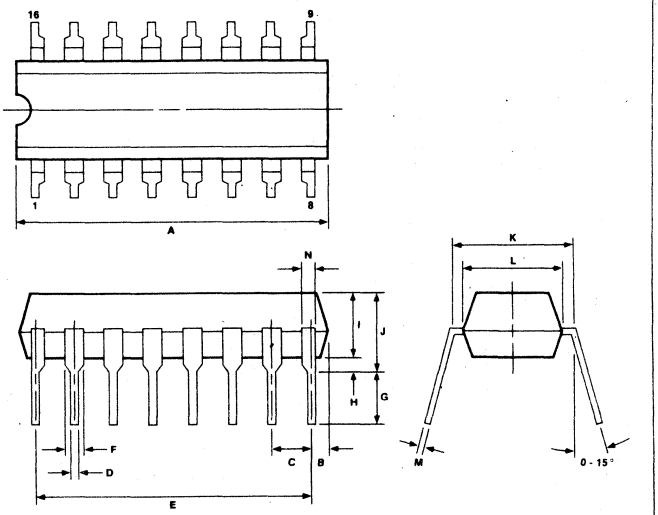


83-003391B

16-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	20.32 max	0.8 max
B	1.27 max	.05 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	17.78	.70
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

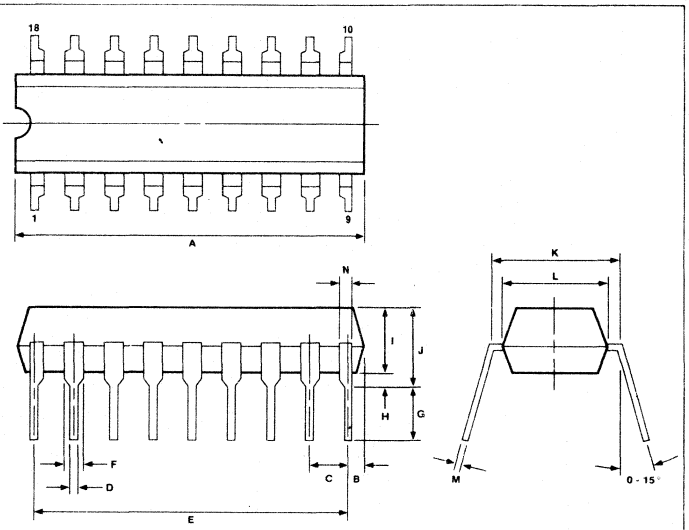


83-001469B

18-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	22.86 max	.9 max
B	1.27 max	.05 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	20.32	.8
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$
N	1.0 min	.039 min

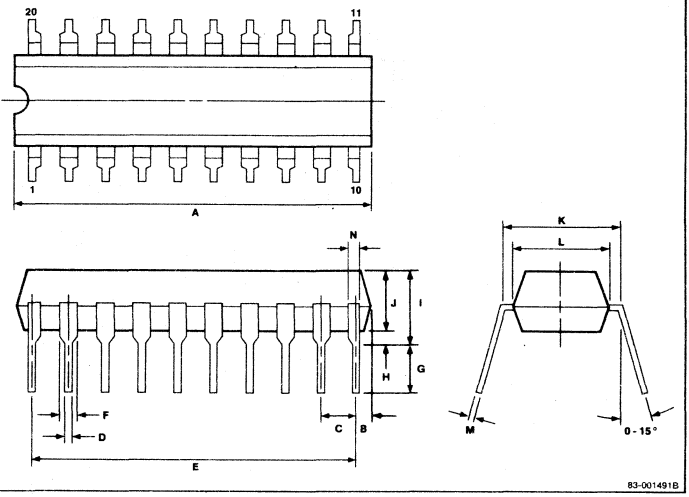
Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



20-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	25.40 max	1.0 max
B	1.27 max	.05 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	22.86	.9
F	1.1 min	.043 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$
N	.9 min	.035 min

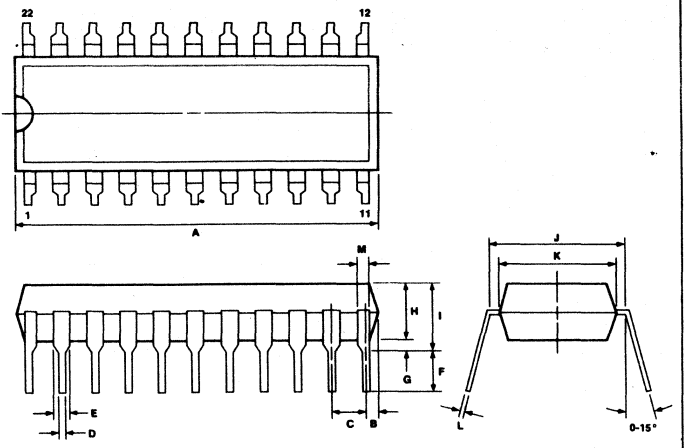
Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



22-Pin Plastic DIP (400 mil)

Item	Millimeters	Inches
A	27.94 max	1.100 max
B	1.27 max	.050 max
C	2.54[TP]	.100[TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	1.2 min	.047 min
F	3.5 ± 0.3	.138 ± .012
G	.51 max	.020 max
H	4.31 max	.170 max
I	5.72 max	.226 max
J	10.16[TP]	.400[TP]
K	8.6	.339
L	$.25^{+.10}_{+.05}$	$.010^{+.004}_{-.003}$
M	0.8 min	.031 min

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "J" to center of leads when formed parallel.

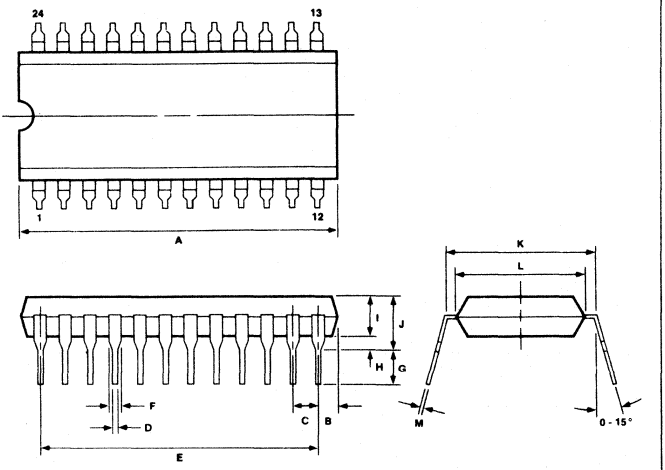


83-003393B

24-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	33.02 max	1.3 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	$.02^{+.004}_{-.005}$
E	27.94	1.1
F	1.2 min	.047 min
G	3.6 ± .3	.138 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.72 max	.226 max
K	15.24 [TP]	.60 [TP]
L	13.2	.52
M	$.25^{+.10}_{-.05}$	$.01^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

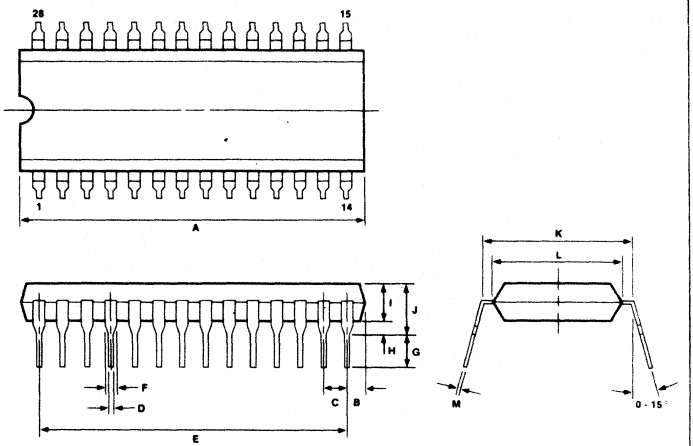


83-001492B

28-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	38.1 max	1.5 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	33.02	1.3
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.72 max	.226 max
K	15.24 [TP]	.60 [TP]
L	13.2	.52
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

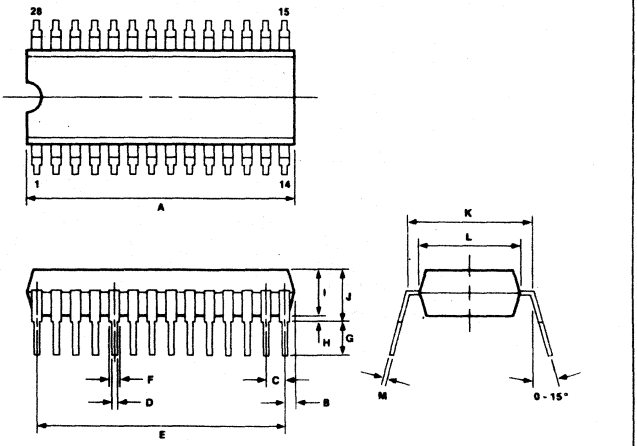


83-001407B

28-Pin Plastic Shrink DIP (400 mil)

Item	Millimeters	Inches
A	28.46 max	1.121 max
B	2.67 max	.106
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.02 $^{+.004}_{-.005}$
E	24.89	.98
F	.9 min	.035 min
G	3.2 ± 0.3	.126 ± 012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

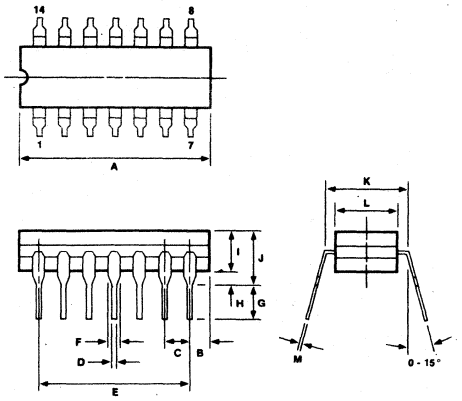


83-0015198

14-Pin Ceramic Package (300 mil)

Item	Millimeters	Inches
A	19.9 max	.78 max
B	2.35	.09
C	2.54 [TP]	.1 [TP]
D	.46	.018
E	15.2	.6
F	1.5	.059
G	3.0 min	.118 min
H	.5 min	.02 min
I	4.58 max	.181 max
J	5.08 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.4	.25
M	.25	.01

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

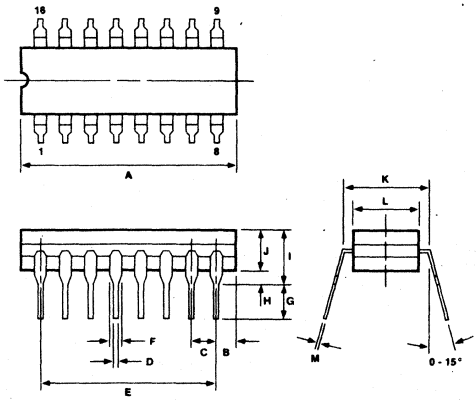


83-001523B

16-Pin Cerdip Package (300 mil)

Item	Millimeters	Inches
A	19.9 max	.784 max
B	1.06	.042
C	2.54 [TP]	.10 [TP]
D	.46 ± .10	.018 ± .004
E	17.78	.70
F	1.5	.059
G	2.54 min	.10 min
H	.5 min	.019 min
I	4.58 max	.181 max
J	5.08 max	.20 max
K	7.62 [TP]	.30 [TP]
L	6.4	.25
M	.25 $^{+.10}_{-.05}$	.0098 $^{+.0039}_{-.0019}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

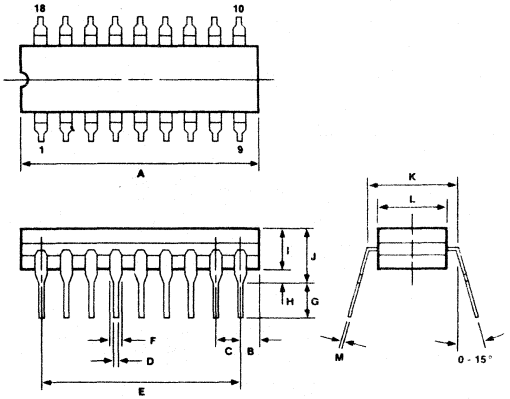


83-001516B

18-Pin Cerdip Package (300 mil)

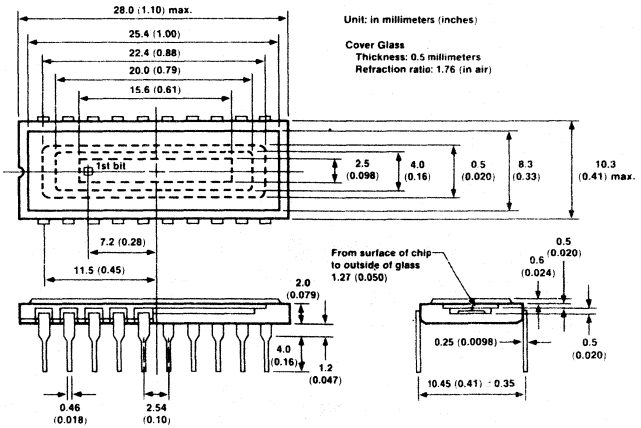
Item	Millimeters	Inches
A	23.2 max	.91 max
B	1.44	.055
C	2.54 [TP]	.10 [TP]
D	.45	.02
E	20.32	.8
F	1.2	.06
G	2.5 min	.1 min
H	.5 min	.02 min
I	4.6 max	.18 max
J	5.1 max	.2 max
K	7.62 [TP]	.3 [TP]
L	6.7	.26
M	.25	.01

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



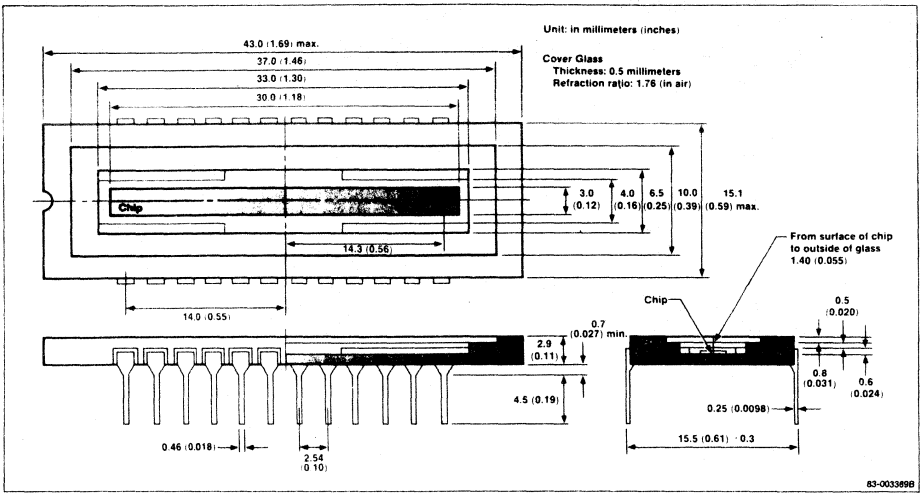
83-001517B

20-Pin Ceramic DIP (μPD795D)

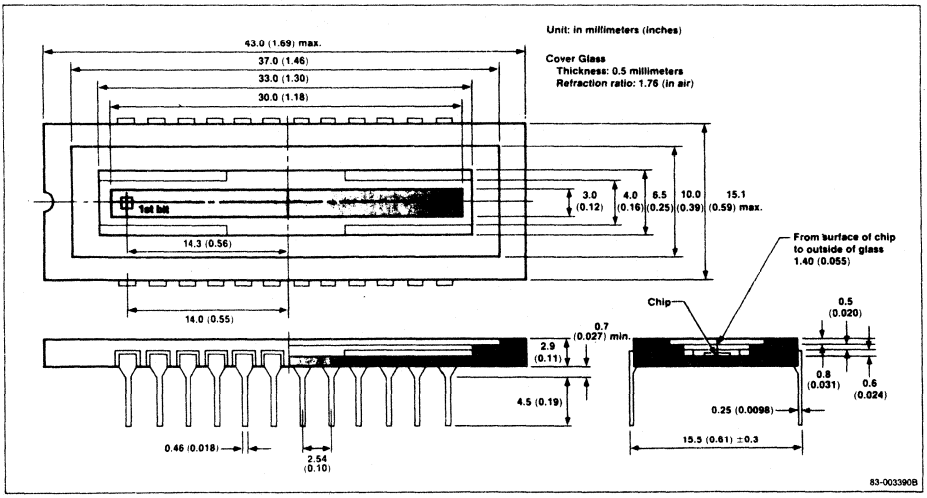


83-003386B

24-Pin DIP (μPD791D)



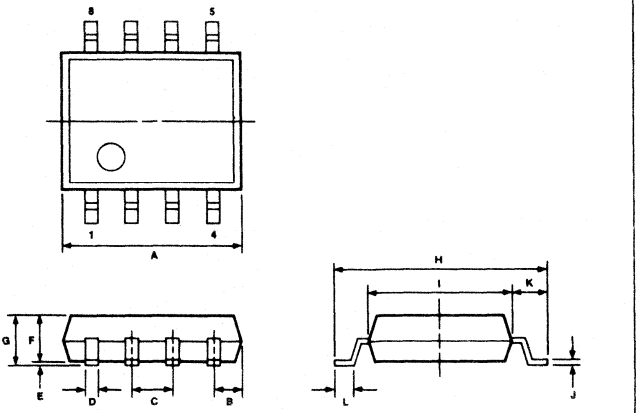
24-Pin DIP (μPD799D)



8-Pin Plastic Minlflat (225 mil)

Item	Millimeters	Inches
A	5.70 max	.22 max
B	.94 max	.037 max
C	1.27 [TP]	.05 [TP]
D	$.40^{+.10}_{-.05}$	$.016^{+.004}_{-.002}$
E	.1 ± .1	.004 ± .004
F	1.49 max	.059 max
G	1.80 min	.071 max
H	6.5 ± .3 [TP]	.256 ± .011 [TP]
I	4.4 max	.173 max
J	$.15^{+.10}_{-.05}$	$.006^{+.004}_{-.002}$
K	1.1 max	.004 max
L	.5 ± .2	.024 ± .008

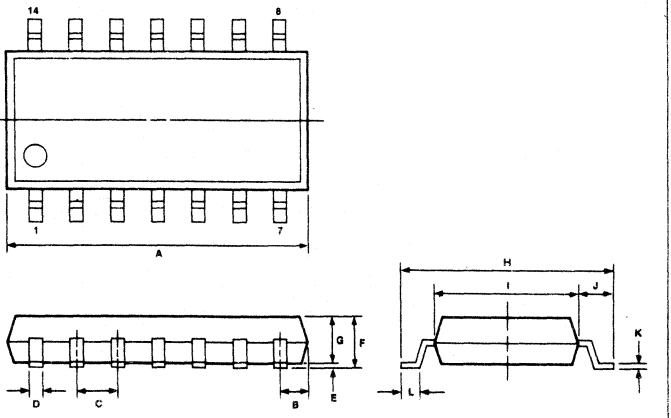
Note: Each lead centerline is located within 0.12 mm (0.005) of its true position (TP) at maximum material condition.



14-Pin Minlflat IC (225 mil)

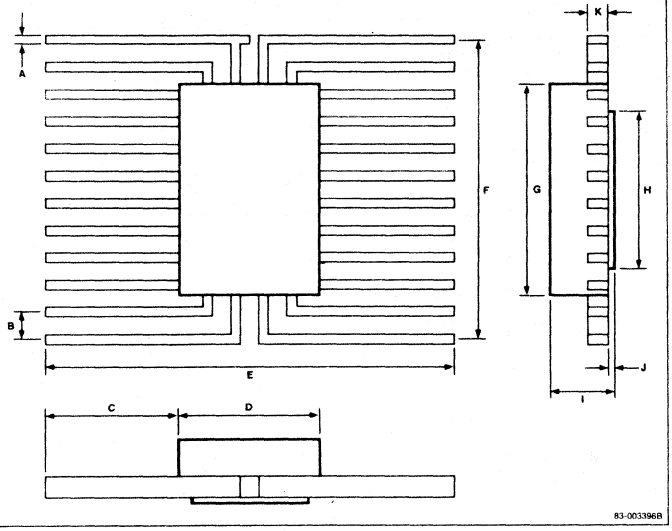
Item	Millimeters	Inches
A	10.46 max	.412 max
B	1.42 max	.056 max
C	1.27 [TP]	.050 [TP]
D	$.40^{+.10}_{-.05}$	$.016^{+.004}_{-.003}$
E	.1 ± .1	.004 ± .004
F	1.8 max	.071 max
G	1.49	.059
H	6.5 ± .3	.256 ± .012
I	4.4	.173
J	1.1	.043
K	$.15^{+.10}_{.05}$	$.006^{+.004}_{-.002}$
L	.6 ± .2	$.024^{+.004}_{-.009}$

Note: Each lead centerline is located within 0.12 mm (0.005) of its true position (TP) at maximum material condition.



24-Pin Ceramic Flatpack B

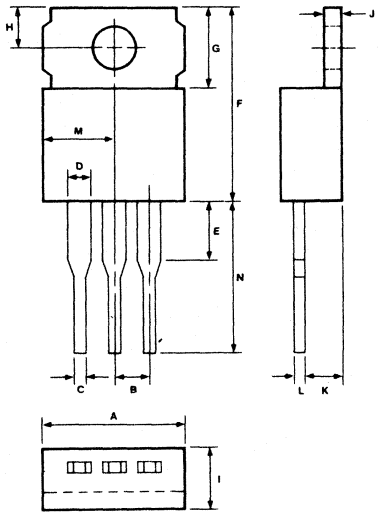
Item	Millimeters	Inches
A	.43 ± .05	.017 ± .002
B	1.27 typ	.050 typ
C	6.35 min	.250 min
D	6.60 ± .15	.260 ± .006
E	19.30 ± .15	.760 ± .006
F	13.97 typ	.550 typ
G	10.11 ± .18	.398 ± .007
H	7.49 ref	.295 ref
I	3.05	.120 max
J	.305	.012 min
K	.13 ± .03	.005 ± .001



3-Pin SIP TO-220

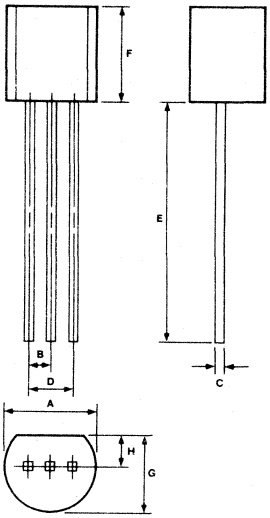
Item	Millimeters	Inches
A	10.66 max	.420 max
B	2.54 [TP]	.100 [TP]
C	$.8^{+.34}_{-.29}$	$.031^{+.013}_{-.011}$
D	1.3	.051
E	6.35 max	.250 max
F	12.7 min	.500 min
G	5.85 min	.230 min
H	$3.0^{+.30}_{-.46}$	$.118^{+.012}_{-.018}$
I	4.82 max	.190 max
J	1.3 ± .2	.051 ± .008
K	$2.8^{+.12}_{-.76}$	$.110^{+.005}_{-.030}$
L	.5 ± .2	.020 ± .008
M	5.33 max	.210 max
N	15.87 max	.625 max

Note: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



3-Pin SIP TO-92

Item	Millimeters	Inches
A	5.2 max	.205 max
B	1.27 max	.067 max
C	.5	.002
D	2.54	.100
E	14 min	.551 min
F	5.5 max	.217 max
G	4.2 max	.165 max
H	1.77 max	.070 max

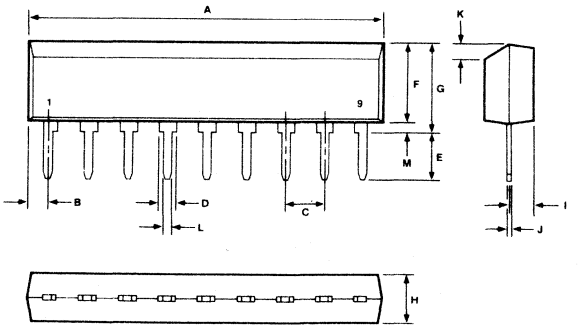


83-003399B

9-Pin Plastic SIP

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.05
C	2.54 [TP]	.100 [TP]
D	1.1 min	.004 min
E	2.9 min	.114 min
F	5.08 max	.200 max
G	5.72 max	.225 max
H	3.0 max	.118 max
I	1.5 max	.059 +.040 −.020
J	.25 +.10 −.05	.006 +.004 −.002
K	1.1	.004
L	.5	.2
M	.51 min	.2 min

Note: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



83-003387B

Thermal Information

The power dissipation capability of semiconductor devices is limited by the maximum allowable junction temperature, the ambient temperature, and the thermal resistance between the junction and the ambient environment.

The temperature difference between the junction and the ambient environment is determined by the following equation.

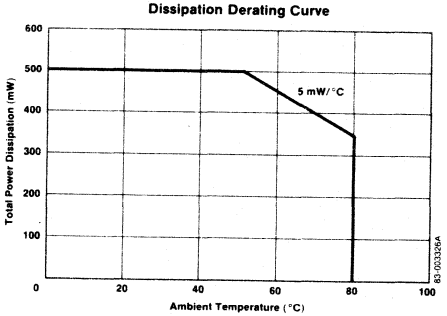
$T_J - T_A = P_D \theta_{JA}$

where T_J = junction temperature, °C
T_A = ambient temperature, °C
P_D = power dissipation, W
θ_{JA} = thermal resistance, junction to ambient, °C/W

The maximum allowable junction temperature is 150 °C, however, the maximum junction temperature of plastic package IC's should be 125 °C because of the storage temperature range limitation.

The dissipation derating curves that follow assume the ambient environment is still air, and that no heat sink is used.

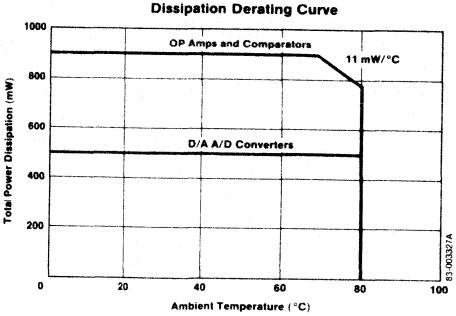
1. 8 Pin Metal Can Package and Cavity DIP



θ_{JA} = 200 °C/W typ. T_J max = 150 °C

The maximum power dissipation value of 500 mW has been fixed considering the practical applications of operational amplifiers and comparators.

2. 14 Pin Through 20 Pin Cavity DIP

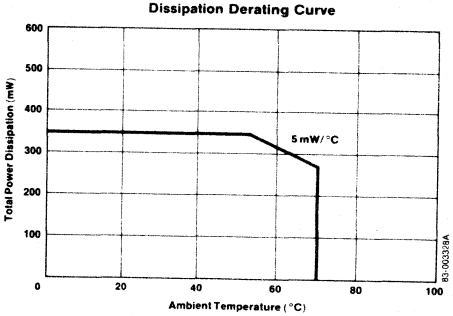


θ_{JA} = 90 °C/W typ. T_J max = 150 °C

The maximum power dissipation value has been fixed considering the practical applications.

Operational Amplifiers and Comparators	900 mW
D/A, A/D Converters	500 mW

3. 8 Pin Plastic Molded DIP

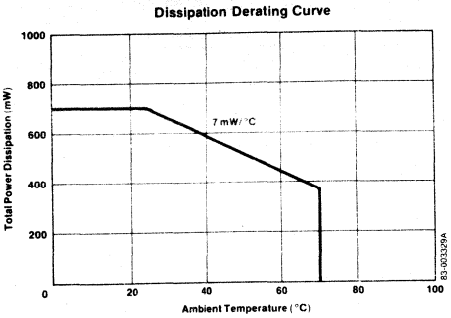


(except for μPC4556C, μPC4557C, μPC4560C, μPC1555C)

θ_{JA} = 200 °C/W typ. T_J max = 125 °C

The maximum power dissipation value of 250 mW has been fixed considering the practical applications of operational amplifiers and comparators.

4. *8 Pin Plastic Molded DIP*



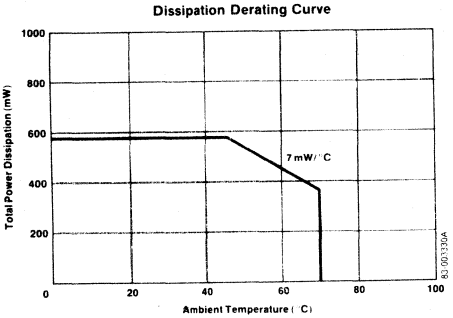
(For μPC4556C, μPC4557C, μPC4560C, μPC1555C)

θ_{JA} = 140 °C/W typ. T_J max = 125 °C

The maximum power dissipation value has been fixed considering the maximum junction temperature and the practical applications of those IC's.

μPC4556, μPC4557, μPC4560C	700 mW
μPC1555C	600 mW

5. *14 Pin Plastic Molded DIP*



θ_{JA} = 140 °C/W typ. T_J max = 125 °C

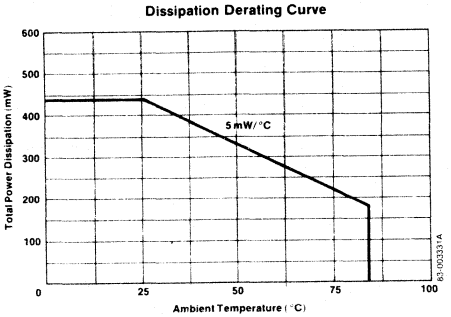
The maximum power dissipation value of 570 mW has been fixed considering the practical applications of operational amplifiers and comparators.

6. Miniflat Package

When the miniflat IC's are mounted on a hybrid IC, the heat radiation through the leads is increased. When resin coated, the heat radiation through the environment is further increased. As a result, the thermal resistance in the mounted state is much smaller than in element form alone.

It is suggested that the heat dissipation in actually mounted condition be fully investigated.

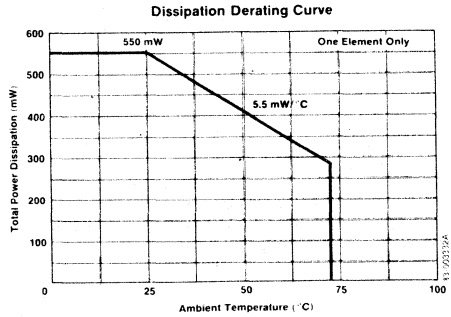
6A. *8 Pin Mini flat Package*



θ_{JA} = 220 °C/W typ. T_J max = 125 °C

The maximum power dissipation value of 440 mW has been fixed considering the maximum junction temperature and the practical applications of miniflat IC's.

6B. *8 Pin Mini flat Package*



θ_{JA} = 180 °C/W typ. T_J max = 125 °C

The maximum power dissipation value of 550 mW has been fixed considering the maximum junction temperature and the practical applications of miniflat IC's.

Taping Specifications

Tape and reel shipping has been used for many years in Japan for shipping surface mount transistors and capacitors. Currently, 75% of surface mount transistors are shipped via this method. Tape and reel specifications, formally established by Japanese Standard RC-1009A for 12 mm tape, has now been expanded to include surface mount ICs.

Surface mount technology in the United States has recently come of age, and in May of 1985 the EIA developed Standard EIA481 for Embossed Tape and Reel Packaging. NEC has adjusted the current Japanese standard to comply with EIA481, and is now shipping surface mount devices to this specification.

Because of the need for electrostatic packaging, NEC chose to manufacture the tape using carbon/PVC material. This type of "filler mixed" plastic is difficult to emboss, thus the actual tape manufacturing is done by the Sumitomo Bakelite Corp in Japan.

The actual manufacturing process is shown in Figure 1. First, rolled sheet material is slittized and embossed. Next, the sprocket holes are punched, and aligned with the embossed pockets to a tolerance of ±50 microns. Finally, the pocket holes are punched, and the tape is cut to length and put on the reel.

Specifications:
NEC's embossed tape is manufactured to EIA481 specifications with special attention paid to dimensional accuracy. See Table 1 and Figure 2. Table 2 and Figure 3 show Reel Dimensions. Figure 4 illustrates the Tape End Configurations. Figure 5 shows component placement in the tape pockets. Table 3 gives the device package-to-tape width specifications. Figures 6, 7 and 8 show the tape and reel specifications for the specialized case of 8, 14 and 16-pin miniflats.

Figure 1. Manufacturing Processes of Embossed Carrier Tape

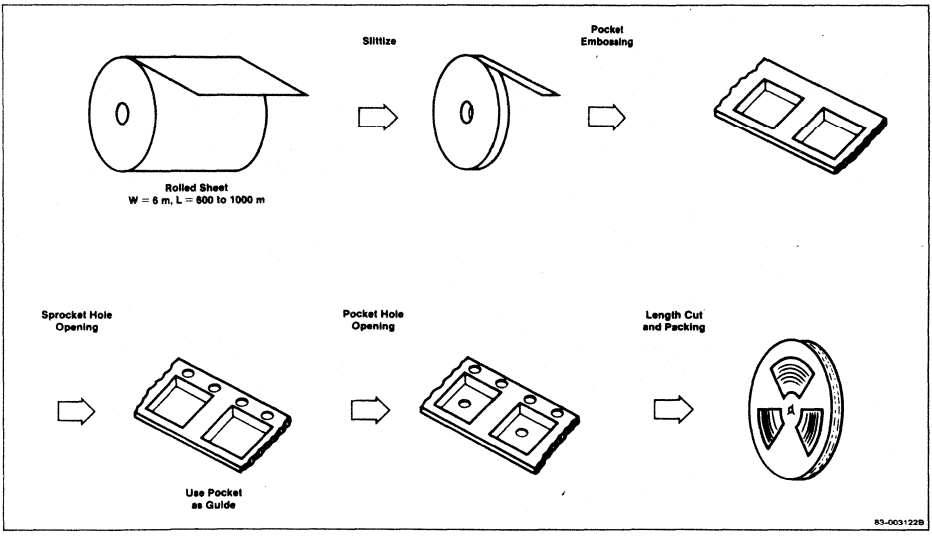


Table 1. 8, 12, 16, 24 mm Embossed Tape

Tape Size	D	E	P_0	t (Max.)	A_0, B_0, K_0	
8, 12, 16, 24 mm	$1.5^{+0.10}_{-0.0}$ ($.059^{+.004}_{-0.01}$)	1.75 ± 0.10 (.069 ± .004)	4.0 ± .10 (.157 ± .004)	0.400 (.016)	See Note 1 Table 2	Constant Dimensions

Tape Size	B_1 Max.	D_1 Min.	F	K Max.	P_2	R Min.	W	
8 mm	4.2 (.165)	1.0 (.039)	3.5 ± 0.05 (.138 ± .002)	2.4 (.094)	2.0 ± 0.05 (.079 ± .002)	25 (.984)	8.0 ± .30 (.315 ± .012	Variable Dimensions
12 mm	8.2 (.323)	1.5 (.059)	5.5 ± 0.05 (.217 ± .002)	4.5 (.177)		30 (1.181)	12.0 ± .30 (.472 ± .012)	
15 mm	12.1 (.476)		7.5 ± 0.10 (.295 ± .004)	6.5 (.256)	2.0 ± 0.10) (.079 ± .004)	40 (1.575)	18 ± .30 (.630 ± .012)	
24 mm	20.1 (.791)		11.5 ± 0.10 (.453 ± .004)			50 (1.969)	24 ± .30 (.945 ± .012)	

	P					
Tape Size	4.0 ± 0.10 (.157 ± .004)	8.0 ± 0.10 (.315 ± .004)	12.0 ± 0.10 (.472 ± .004)	16 ± 0.10 (.630 ± .004)	20 ± 0.10 (.787 ± .004)	24 ± 0.10 (.945 ± .004)
8 mm	X					
12 mm	X	X				
16 mm	X	X	X			
24 mm			X	X	X	X

Notes:

1. A_0 B_0 K_0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (.002) min. to 0.50 (.020) max. for 8 mm tape, 0.05 (.002) min. to 0.65 (.026) max. for 12 mm tape, 0.05 (.002) min. to 0.90 (.035) max for 16 mm tape and 0.05 (.002) min. to 1.00 (.039) max. for 24 mm tape and larger. The component cannot rotate more than 20° within the determined cavity, see below.
2. Tape and components shall pass around radius "R" without damage.

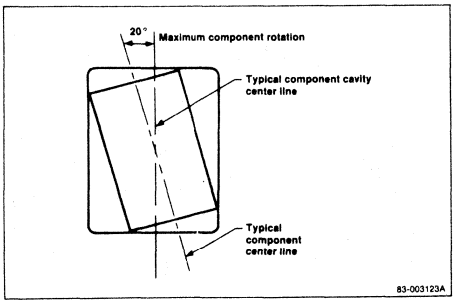


Figure 2. Embossed Carrier Dimensions

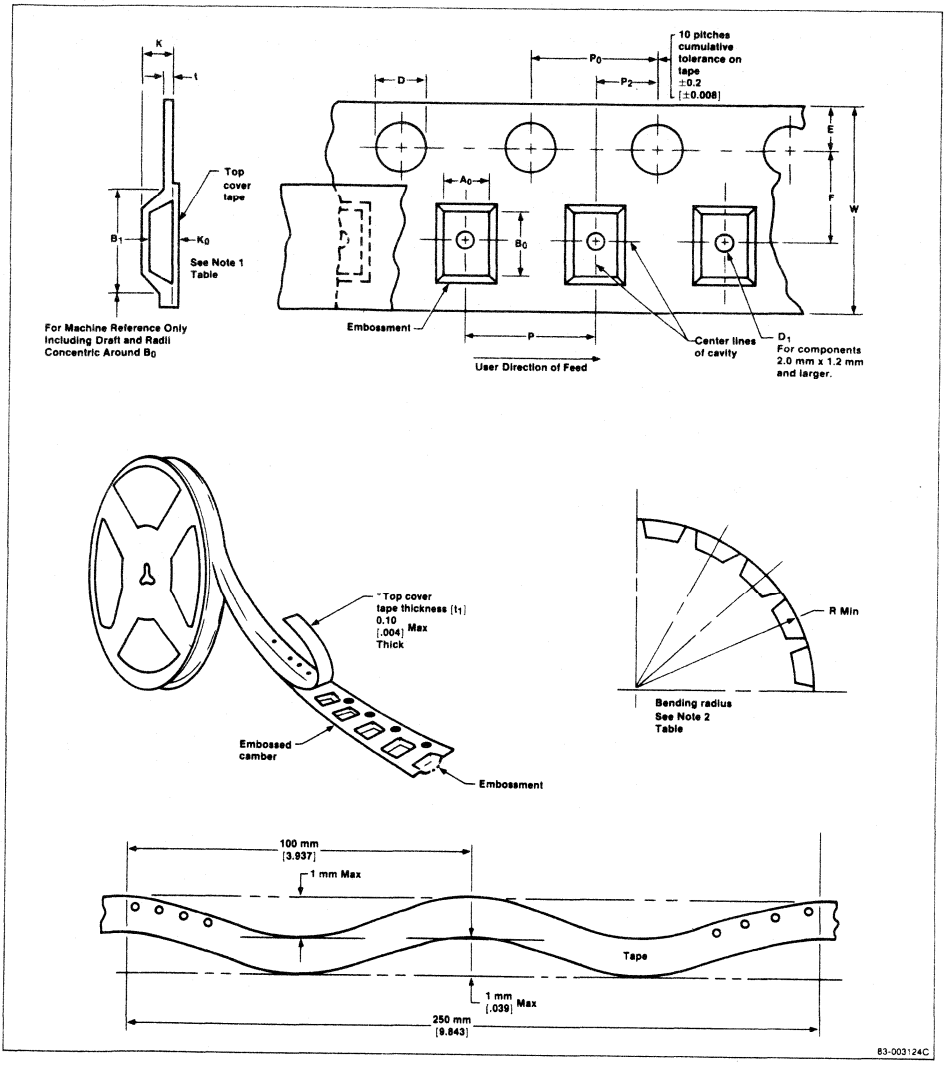


Figure 3. Reel Dimensions

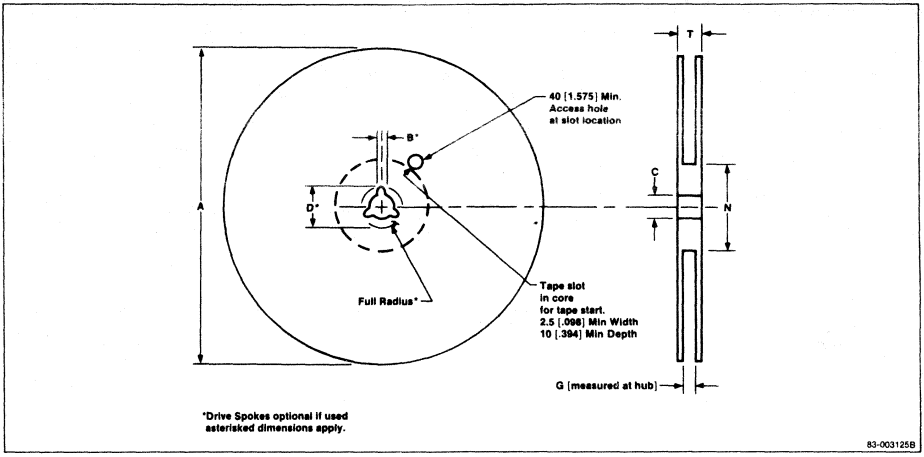


Table 2. Reel Dimensions

Tape Size	A Max.	B Min.	C	D Min.	N Min.	G	T Max.
8 mm	330 (12.992)	1.5 (.059)	13.0 ± 0.20 (.512 ± .008)	20.2 (.795)	50 (1.1969)	$8.4^{+1.5}_{-0.0}$ ($.331^{+.008}_{-0.0}$)	14.4 (.567)
12 mm	330 (12.992)					$12.4^{+2.0}_{-0.0}$ ($.488^{+.078}_{-0.0}$)	18.4 (.724)
16 mm	380 (14.173)					$16.4^{+2.0}_{-0.08}$ ($.646^{+.078}_{-0.0}$)	22.4 (.882)
24 mm						$24^{+2.0}_{-0.08}$ ($.961^{+.078}_{-0.00}$)	30.4 (1.197)
32 mm						$32.4^{+2.0}_{-0.0}$ ($1.276^{+.078}_{-0.00}$)	
44 mm						$44.4^{+2.0}_{-0.0}$ ($1.748^{+.078}_{-0.00}$)	
55 mm	609 (23.976)				100 (3.937)	$58.4^{+2.0}_{-0.0}$ ($2.220^{+.078}_{-0.0}$)	

Metric dimensions will govern.
English measurements rounded and for reference only.

Figure 4. Tape End Configurations

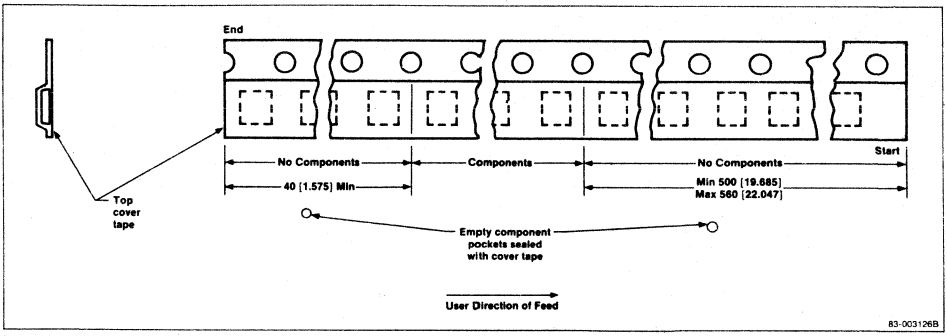


Figure 5. SO-IC Devices

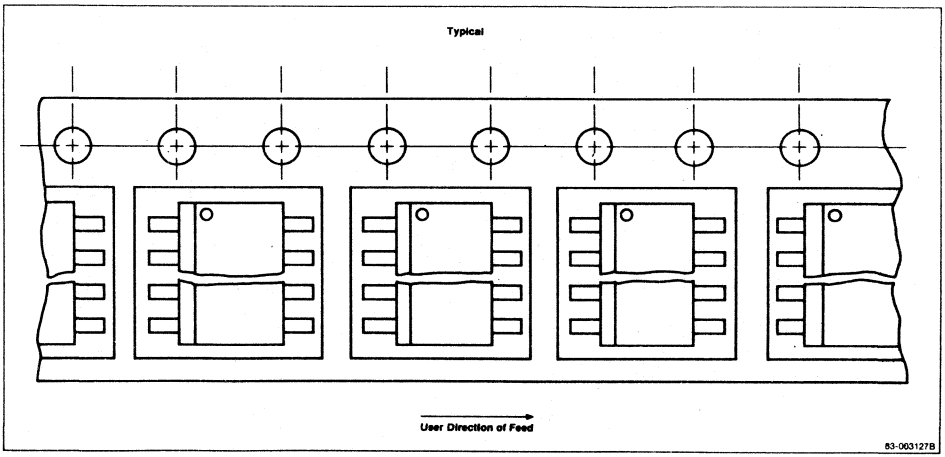
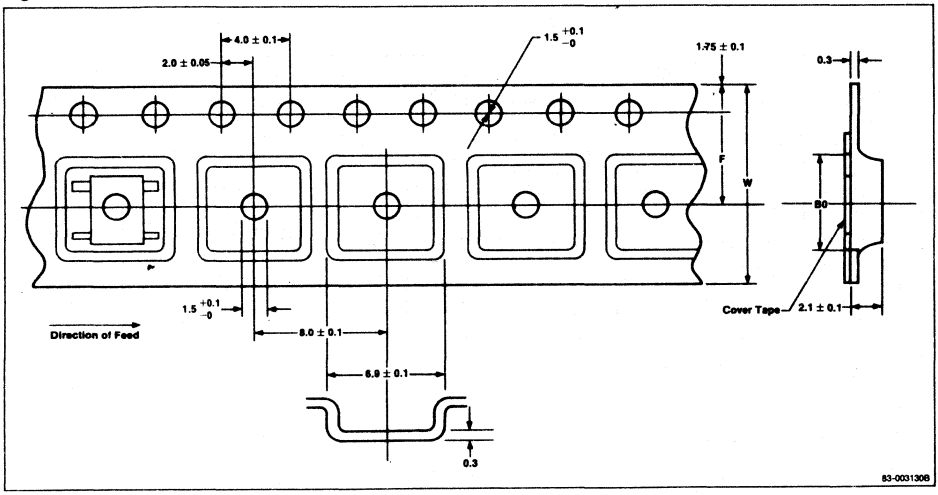


Table 3. SO-IC Devices

Component		Tape Size mm (W)	Part Pitch (P)
SO-IC 225 mil MF	8	12	8
	14	16	8
	16	16	8
SO-IC 375 mil MF	14L	16	12
	16L	16	12
	20L	24	12
	24L	24	12
	28L	24	12
PCC	18	24	12
	20	16	12
	28	24	16
	44	32	24
PCC	52	32	24
	68	44	32
	84	44	36
	100	44	40
	124	56	48

Figure 6. Embossed Carrier Dimensions



Package	B_0	W	F
8p SMF	5.4 ± 0.1	12.0 ± 0.3	5.5 ± 0.1
14, 16p SMF	10.45 ± 0.1	16.0 ± 0.3	7.5 ± 0.1

SMF: 225 mil Miniflat

	8p SMF	14, 16 SMF
W	$12.4^{+2.0}_{-0}$	$16.4^{+2.0}_{-0}$
T	18.4 Max	22.4 Max

SMF: 225 mil Miniflat

Figure 7. Reel Size

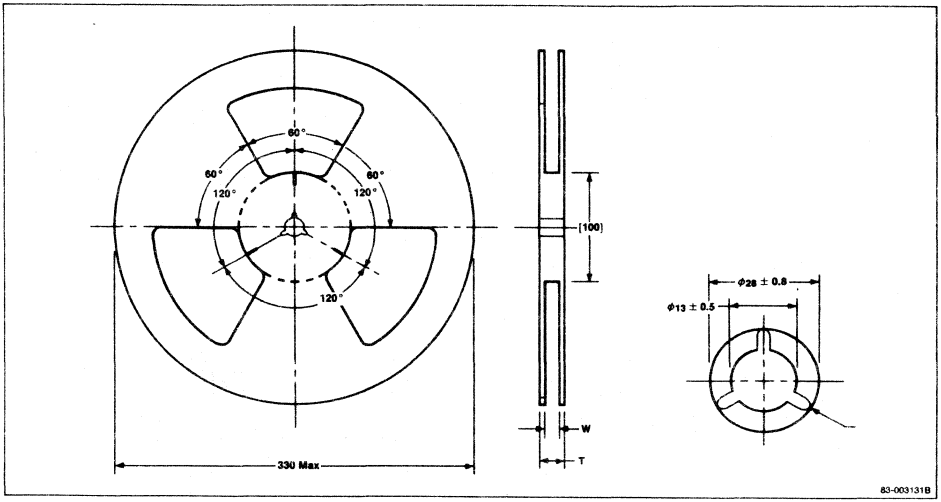
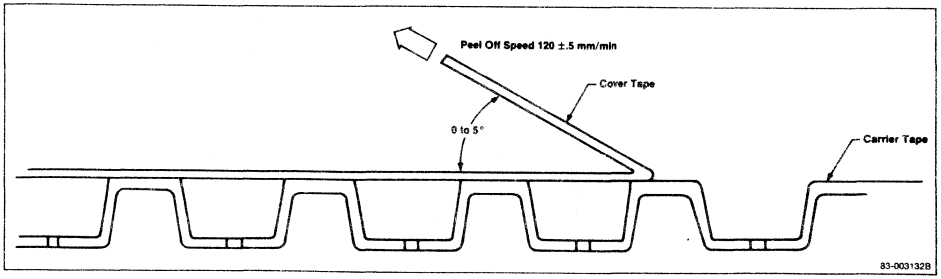
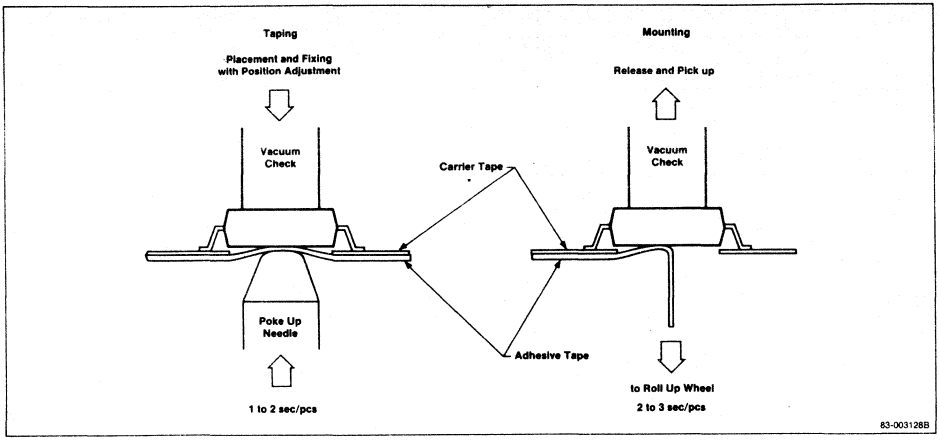
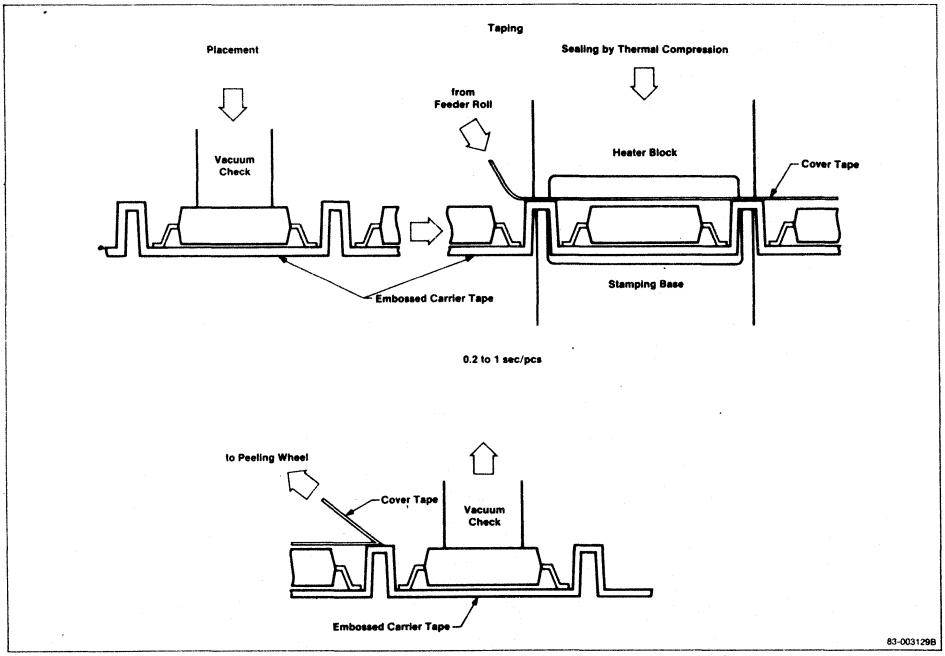


Figure 8. Cover Tape Peel Strength: 40 ± 25 g




Taping
Placement and Fixing with Position Adjustment
Vacuum Check
Poke Up Needle
1 to 2 sec/pcs
Carrier Tape
Adhesive Tape
Mounting
Release and Pick up
Vacuum Check
to Roll Up Wheel
2 to 3 sec/pcs
83-003128B


Taping
Placement
Vacuum Check
from Feeder Roll
Sealing by Thermal Compression
Heater Block
Cover Tape
Embossed Carrier Tape
Stamping Base
0.2 to 1 sec/pcs
to Peeling Wheel
Cover Tape
Vacuum Check
Embossed Carrier Tape
83-003129B

Surface Mount Information

Structure

The designation for industrial linear IC (ILIC) in the miniflat package is "G2." Figure 1 shows a cutaway view of the miniflat G2 package. The die (chip) is mounted to the center lead frame island, with bonding pads to the external leads.

The lead frame is made from 42 Alloy with silver (Ag) paste used for die attachment. The body is high-purity molded epoxy for high reliability.

Figure 2 shows the package cross section.

Package Outline

In 1981, the EIAJ (Electronic Industry Association of Japan) set the standards for Surface Mount ICs. They required that devices manufactured in Japan attain higher resistance to environmental factors (humidity, shock, and vibration) than existing Small Outline Integrated Circuit (SOIC) devices. The resulting package is known as the 225-Mil S.O. Specification.

Figure 3 illustrates the difference between the NEC miniflat (G2) and the S.O. type package.

The body or molded portion of the NEC miniflat is 4.4 mm wide compared to 4.0 mm for the S.O. package. The lead bend of the NEC miniflat adds an additional 0.1 mm, for a net difference of approximately 0.5 mm in overall footprint width (miniflat vs. SOIC). All other dimensions (such as lead pitch, length, and spacing) are the same.

The larger package size of the NEC miniflat allows a larger die to be mounted in 8- and 14-pin packages, (e.g. BIFET op amp), which increases the variety of circuits available in the G2 package. See Package Information Section for the outline dimensions of 8-pin and 14-pin G2 packages.

Figure 1. Internal Structure (8-Pin Type)

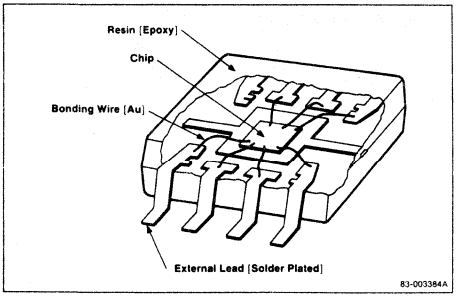


Figure 2. Cross Section of a Miniflat IC

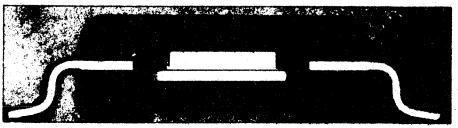
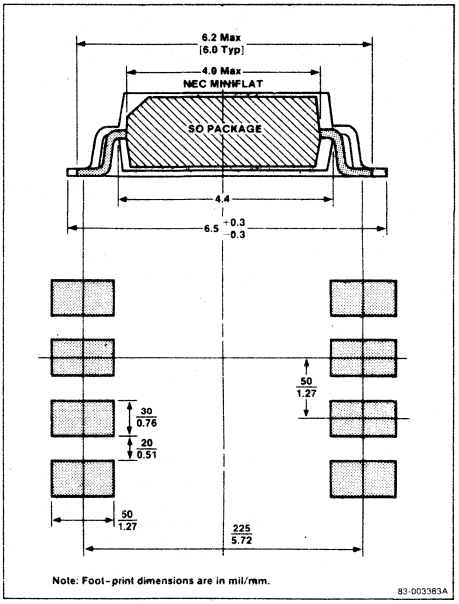


Figure 3. Compatible Footprint Pattern for NEC Miniflat IC and SOIC



Handling Techniques

To work with the NEC miniflat IC without jeopardizing the quality and reliabilty, it is necessary to exercise more care than when handling standard DIP ICs.

Environmental conditions and handling precautions for the NEC miniflat IC family are described below.

Circuit Design

The electrical characteristics of the NEC miniflat IC are guaranteed the same as those of standard DIP ICs.

Since heat radiation is improved when the IC is mounted on the substrate, power dissipation P_T can be changed in actual use. However, the degree of change

largely depends on the method of mounting (size of substrate, coating method, etc). Therefore, full evaluation of the mounted board should be made in advance.

Total Power Dissipation and Thermal Resistance

Figures 4 and 5 show the total power dissipation characteristics of the NEC miniflat IC family.

As shown in the figures, thermal resistance for a single element is approximately 180°C/W for the 14-pin IC, and approximately 220°C/W for the 8-pin IC.

When mounted on a hybrid IC or PW-board, the heat radiation through the leads is increased. With resin coating, the heat radiation through the resin to the environment is further increased. As a result, the thermal resistance in the mounted state is much lower.

It is suggested that the heat dissipation in actual finished mountings be fully analyzed prior to production.

Figure 4. P_T–T_j Characteristic (8-Pin Type)

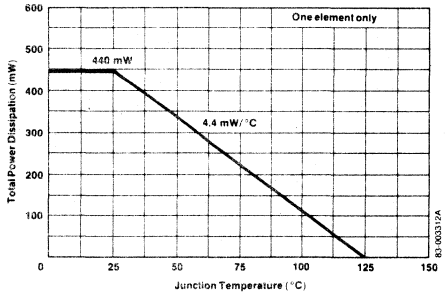
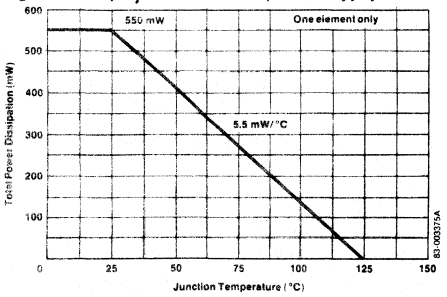


Figure 5. P_T–T_j Characteristic (14-Pin Type)



Soldering and Flux Temperature

Exposure to high temperatures over time should be carefully monitored to insure prolonged reliability. As An Absolute Maximum Rating, exposure to the following must not exceed 260°C for 10 seconds.

- Solder dipping
- Soldering iron
- High-temperature atmosphere

Rosin flux (pine resin) is recommended as soldering flux.

NOTE: Avoid flux containing chlorine. Residual chlorine after cleaning may affect reliability.

Cleaning

Flux should be thoroughly removed after soldering. Alcohol, Chlorocene, and Freon are all acceptable solvents; however, prolonged immersion in these solvents may remove printed markings.

Ultrasonic cleaning can also be applied if other components mounted on the same board can withstand it.

Protection Against Humidity

Being super-miniaturized and employing a thinner plastic than standard DIP ICs, the miniflat IC has shorter leakage paths and requires much more protection against humidity.

Generally, anti-humidity protection is provided by resin coating after mounting on board. Examples of the process are described below.

- When sealed in an airtight package, no precoating is necessary.
- When sealed with resin, a buffer coating may be required as the resin contraction may exert stress on ICs when sealing. Sufficient evaluation should be made on the actual board.
  For buffer coating, the use of resin with a certain degree of viscosity is suggested.

Please consult the resin manufacturers for appropriate encapsulation resin and coating materials.

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